

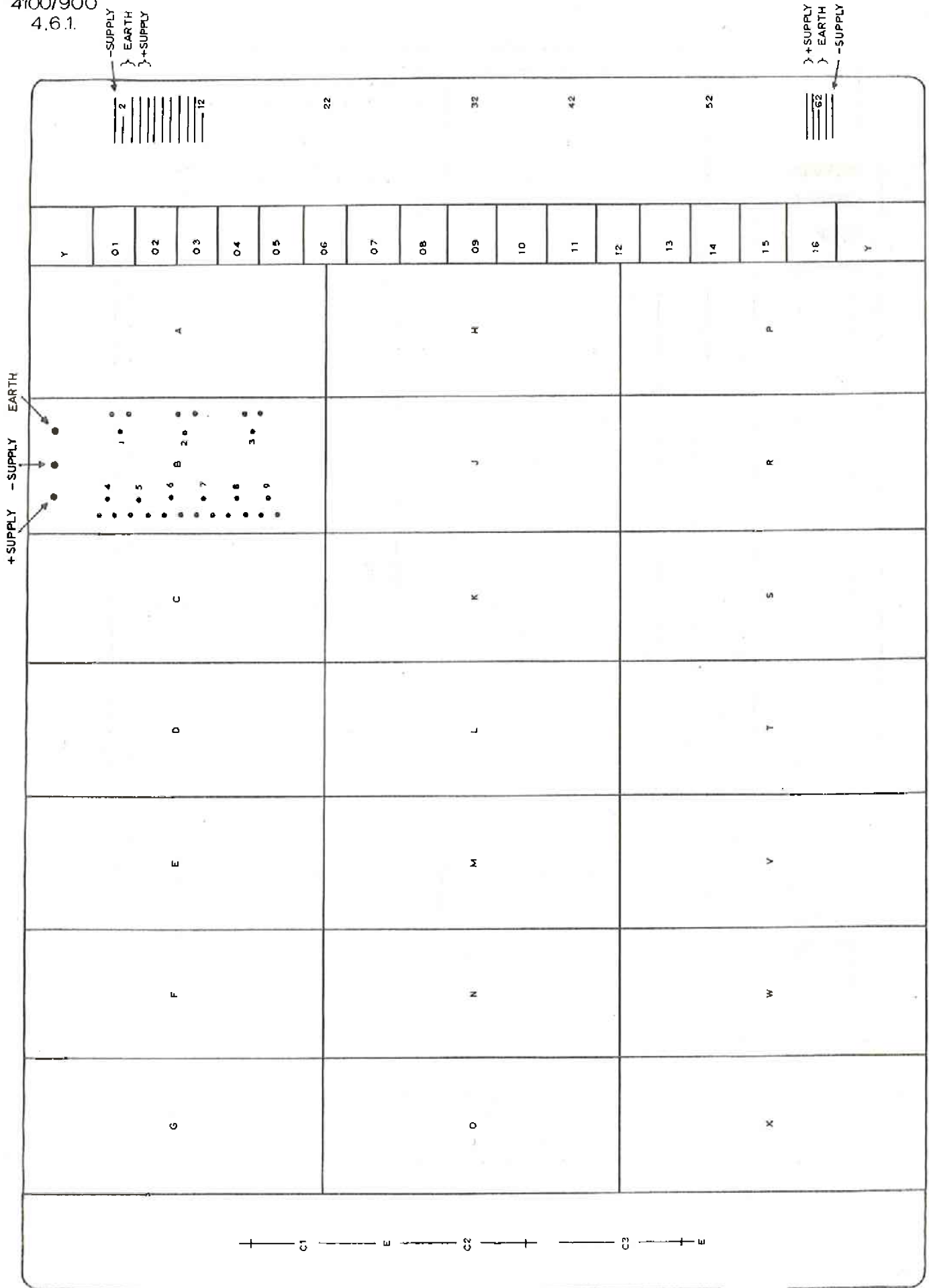
NOTES:

- (1) PAD NUMBERS IN L.S.A AREAS ARE STANDARD
- (2) PINS 33 TO 64 ARE ON OPPOSITE SIDE OF BOARD

TYPICAL DP BOARD (VIEWED FROM L.S.A. SIDE)

Figure 1 (ISSUE B)

4100/900
4.6.1.

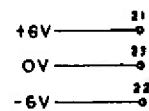
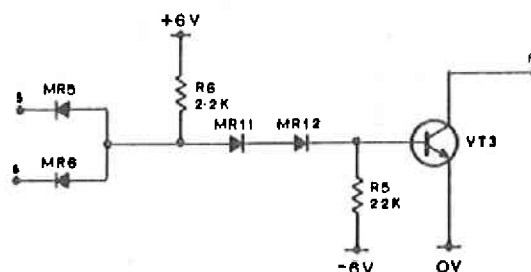
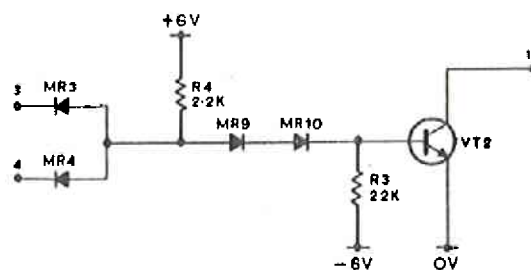
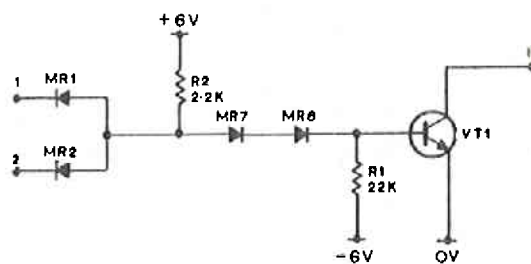
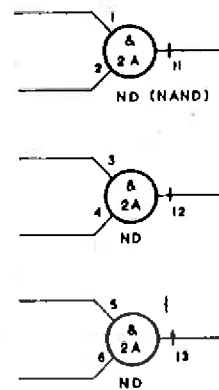
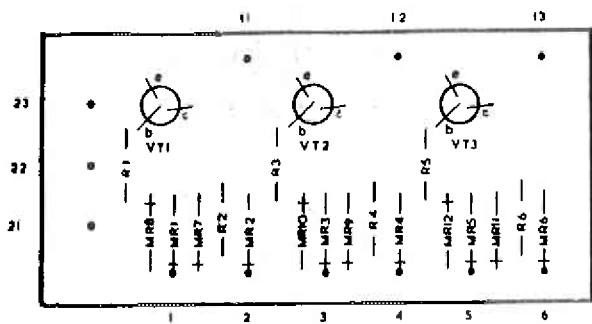


TYPICAL NV BOARD (VIEWED FROM L.S.A. SIDE)

NOTE: PAD NUMBERS IN L.S.A. AREAS ARE NON-STANDARD

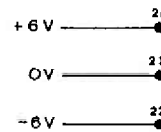
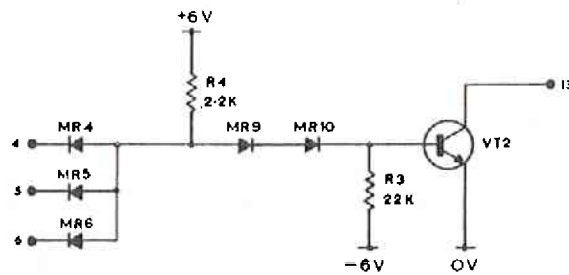
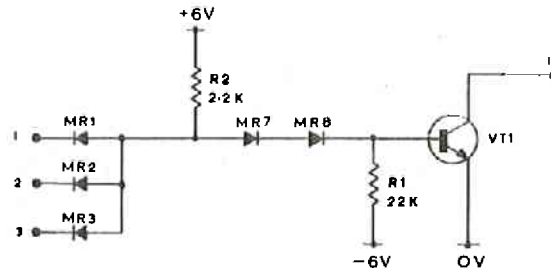
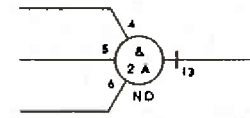
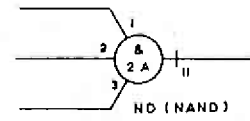
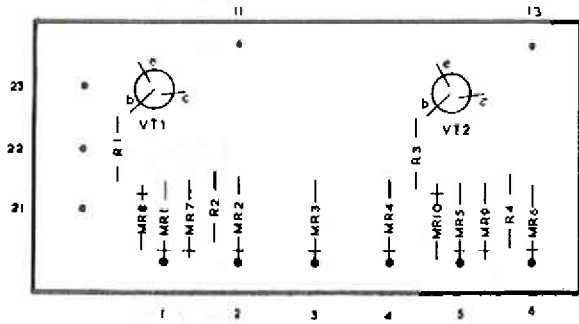
Figure 2 (ISSUE 2)

TRANSISTOR PURCH SPEC CAT NO.
VT1-VT3 PS 218 11008



INPUT LOGIC LEVELS	
'1'	= > 2V
'0'	= < 1V

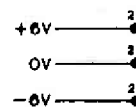
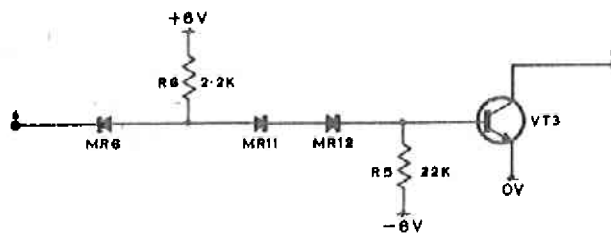
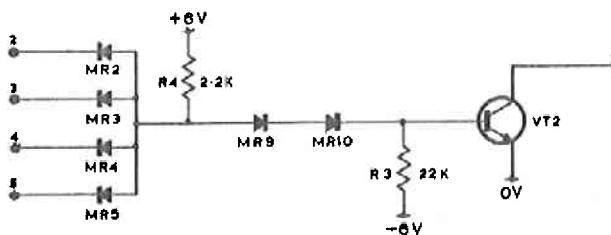
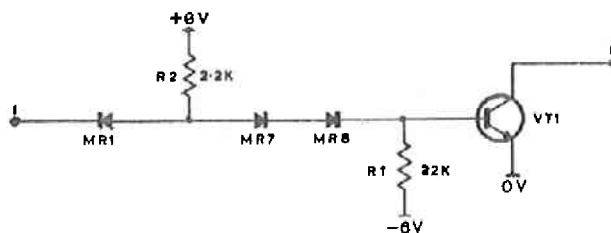
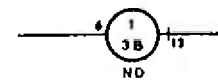
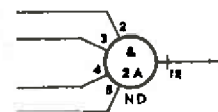
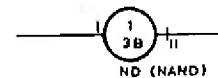
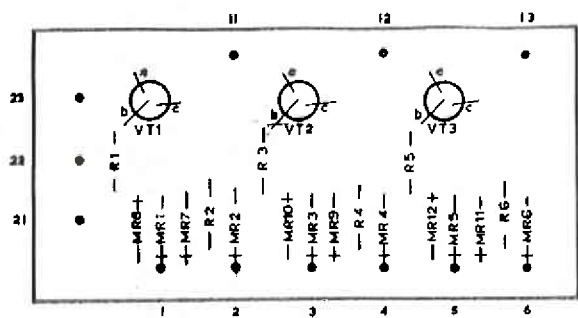
TRANSISTOR PURCH. SPEC. CAT. NO.
VT1 VT2 PS 218 11008



INPUT LOGIC LEVELS	
'1'	= > 2V
'0'	= < 1V

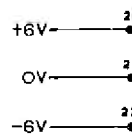
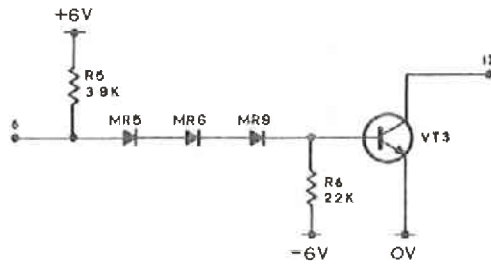
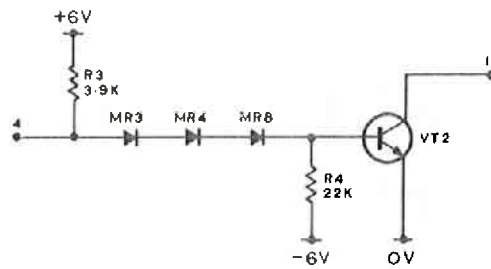
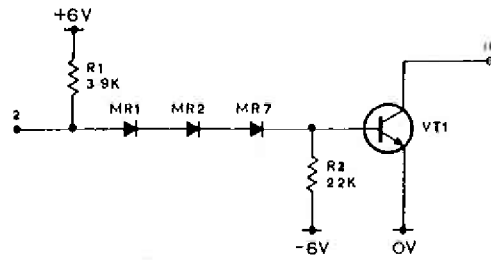
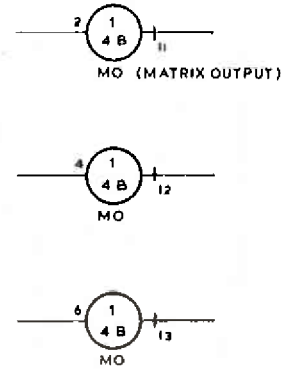
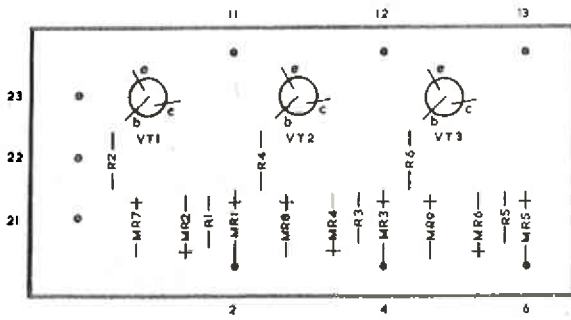
Figure 4 (ISSUE 2)

TRANSISTOR PURCH. SPEC. CAT. No
VT1-VT3 PS 218 1100B



INPUT LOGIC LEVEL	
'1'	> 2V
'0'	< 1V

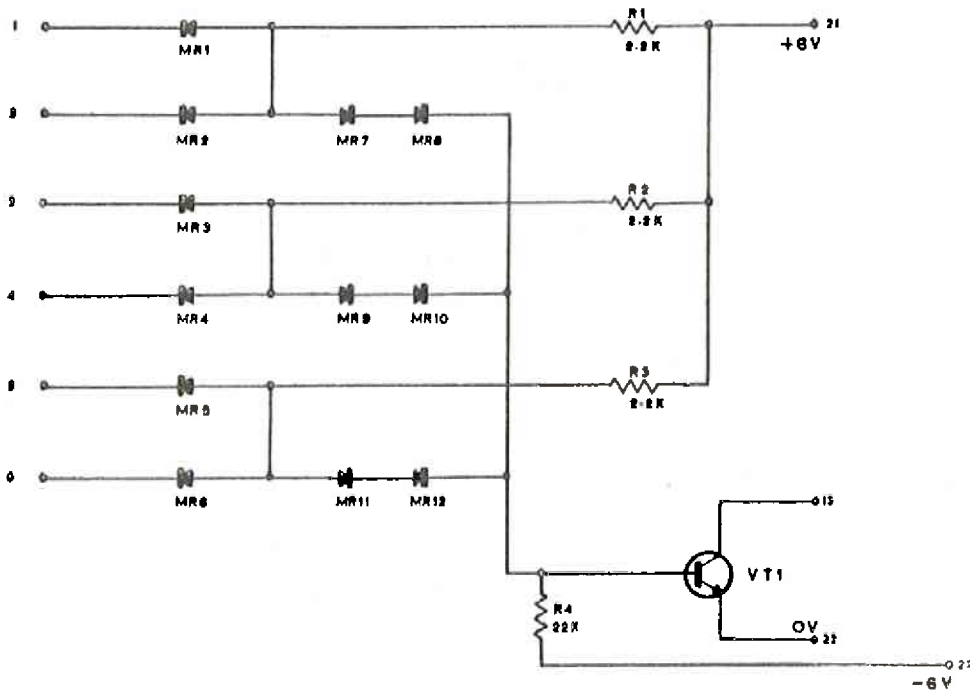
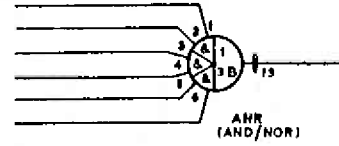
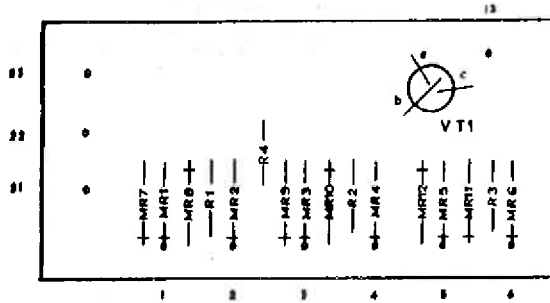
TRANSISTOR PURCH. SPEC. CAT NO.
VT1-VT3 PS 21B 1100B



INPUT LOGIC LEVELS	
1	= > 3V
0	= < 1V

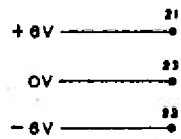
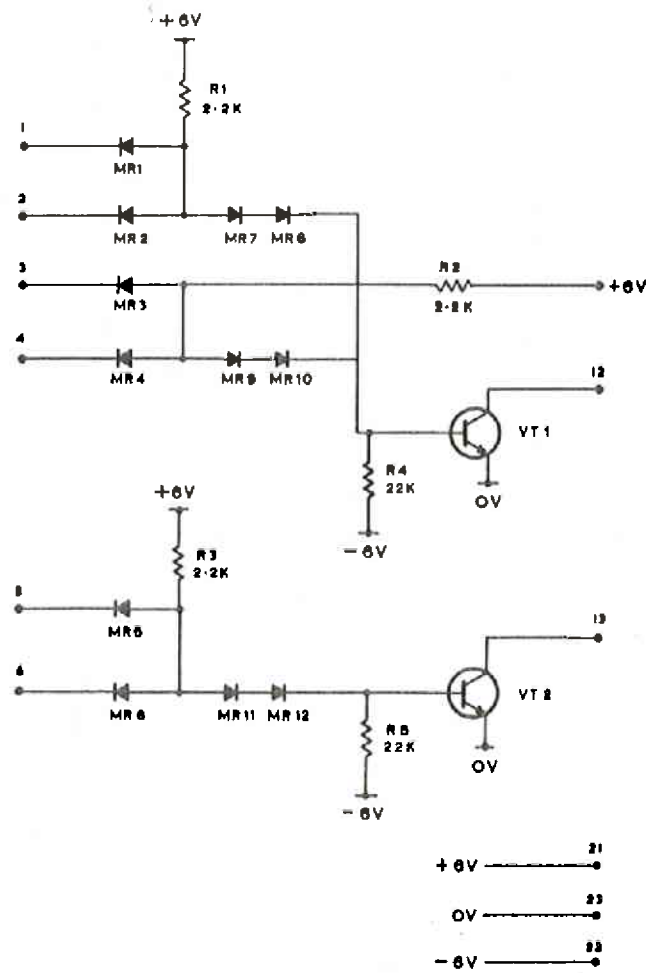
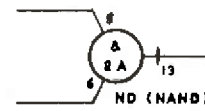
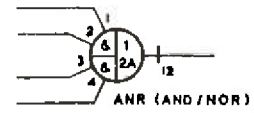
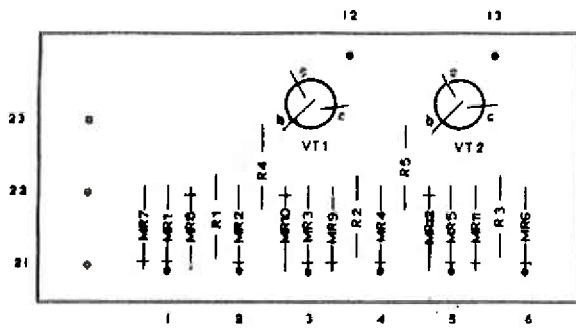
Figure 6 (ISSUE 2)

TRANSISTOR PURCH. SPEC. CAT. NO.
VT1 PS 216 11006



INPUT LOGIC LEVELS
'1' = > 2V.
'0' = < 1V.

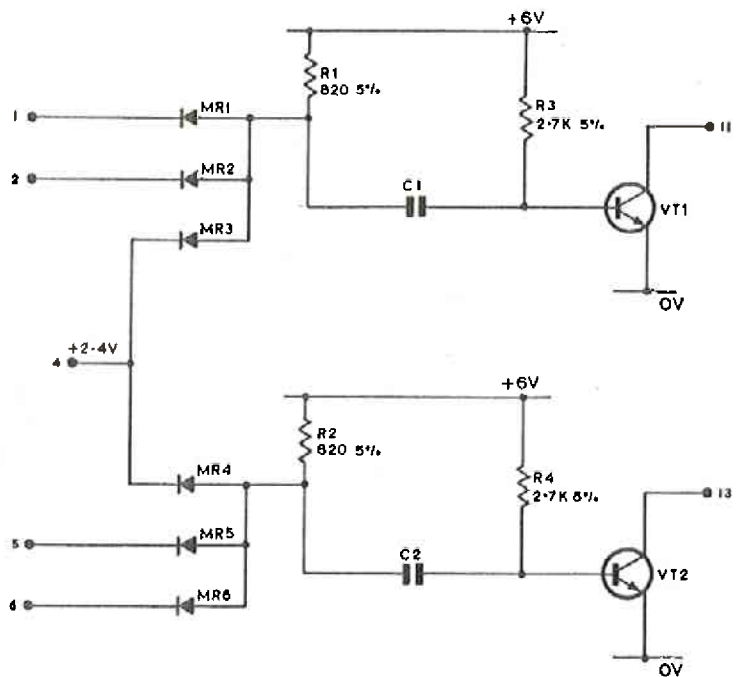
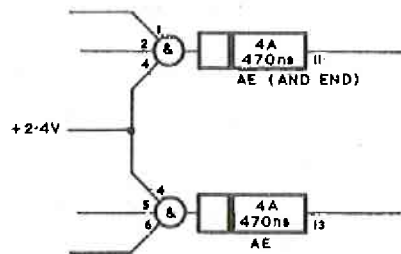
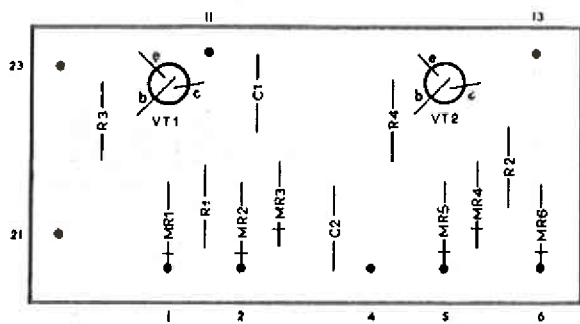
TRANSISTOR PURCH SPEC CAT NO.
VT1, VT2 PS 216 11008



INPUT LOGIC LEVELS	
'1'	= > 2V
'0'	= < 1V

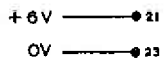
Figure 8 (ISSUE 2)

TRANSISTOR PURCH. SPEC. CAT. NO.
VT1, VT2 PS 218 11008



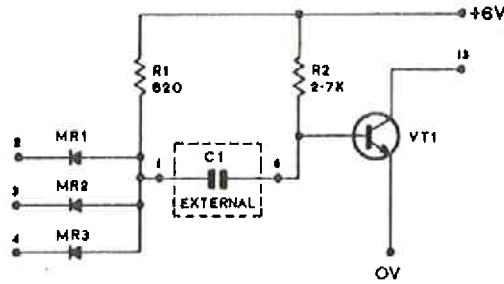
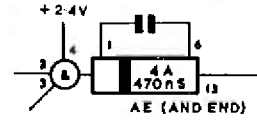
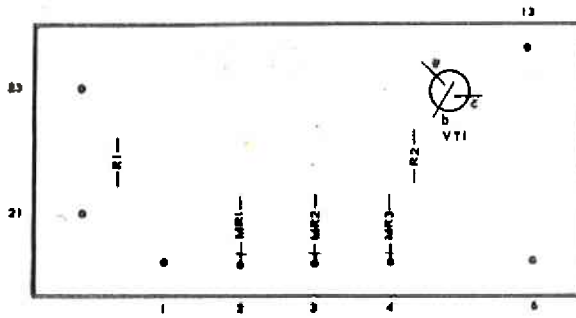
LSA No	C1 (pF)	C2 (pF)
07	100	100
13	330	330
137	220	220
138	470	470
34	100	330

- NOTES:
- (1) OUTPUT PULSE POSITIVE
 - (2) PULSE TRIGGERED BY ANY INPUT REVERTING TO '0' PROVIDING ALL I/P'S HAVE BEEN '1' FOR GREATER THAN $C/2 \text{ ns}$ (WHERE C = CAPACITANCE IN pF)
 - (3) PULSE WIDTH = $C \text{ ns}$ (WHERE C = CAPACITANCE IN pF)



INPUT LOGIC LEVELS	
'1'	= >2V
'0'	= <1V

TRANSISTOR PURCH. SPEC. CAT. NO.
VT1 PS 218 11008

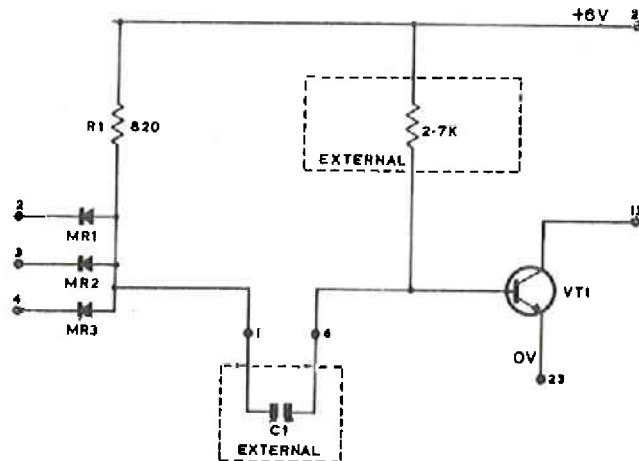
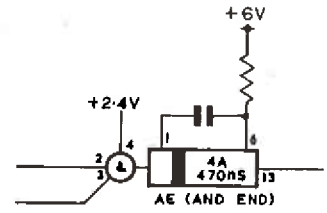
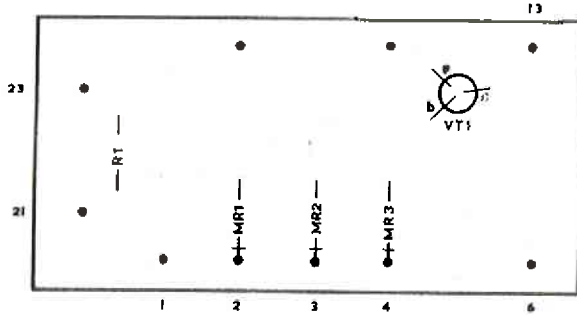


NOTES:

- (1) OUTPUT PULSE POSITIVE.
- (2) PULSE TRIGGERED BY ANY INPUT REVERTING TO '0' PROVIDING ALL '1' HAVE BEEN '1' FOR $> C/2 \text{ ns}$ (WHERE C = CAPACITANCE IN pF).
- (3) PULSE WIDTH $\approx C \text{ ns}$ (WHERE C = CAPACITANCE IN pF).
C1 WILL BE AN EXTERNAL CAPACITOR.

INPUT LOGIC LEVELS	
'1'	$\approx > 2V$
'0'	$\approx < 1V$

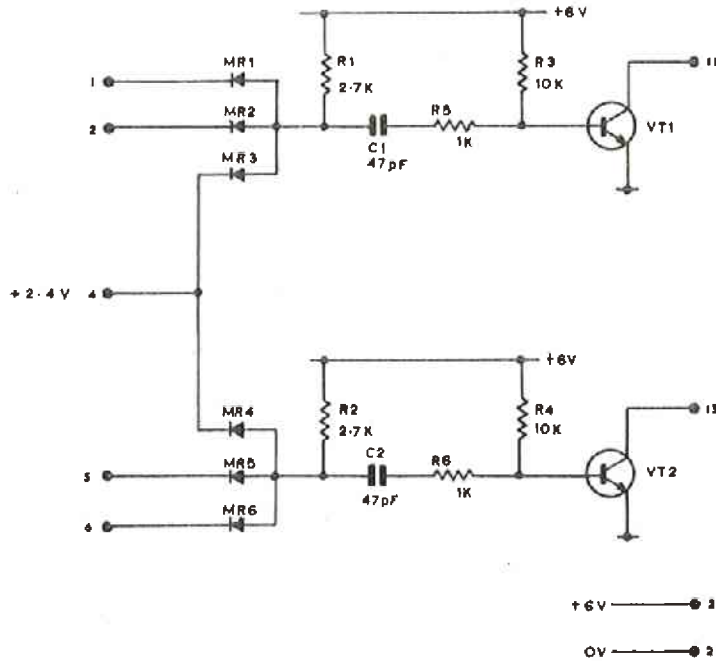
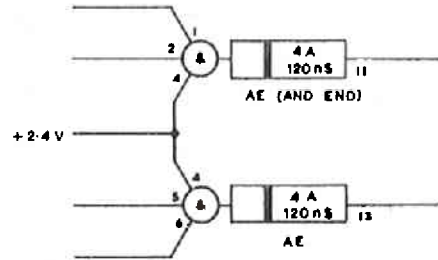
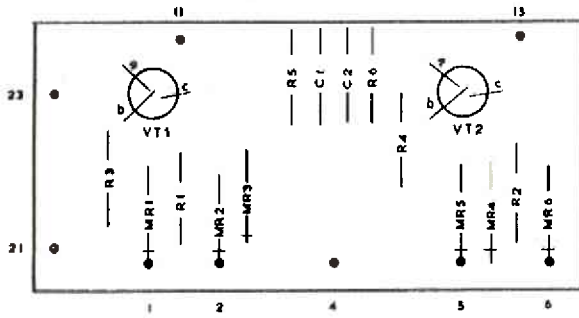
TRANSISTOR PURCH. SPEC. CAT. No
VT1 PS 218 11008



- NOTES:
- (1) OUTPUT PULSE POSITIVE.
 - (2) PULSE TRIGGERED BY ANY INPUT REVERTING TO '0' PROVIDING ALL '1'p's HAVE BEEN '1' FOR $> \frac{1}{2} \tau$
 - (3) PULSE WIDTH $\approx C \tau$ (WHERE C = CAPACITANCE IN pF.)

INPUT LOGIC LEVELS	
'1'	$\geq 2V$
'0'	$< 1V$

TRANSISTOR PURCH. SPEC. CAT. NO.
VT1 VT2 PS 218 11008

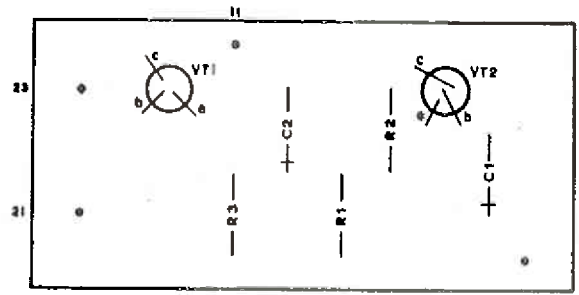
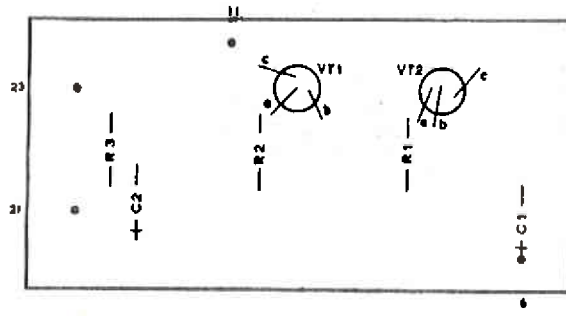


NOTES >

- (1) OUTPUT PULSE POSITIVE
- (2) PULSE TRIGGERED BY ANY INPUT REVERTING TO '0' PROVIDING ALL I/P'S HAVE BEEN '1' FOR GREATER THAN 80 ns.
- (3) PULSE WIDTH = 120 ns \pm 20%.

INPUT LOGIC LEVELS	
'1'	= > 2V
'0'	= < 1V

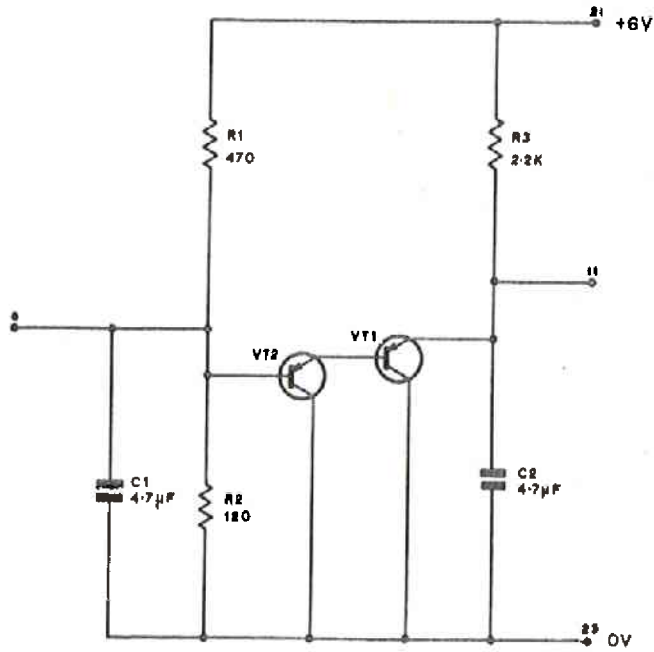
TRANSISTOR CAT. NO.
VT1, VT2 11740



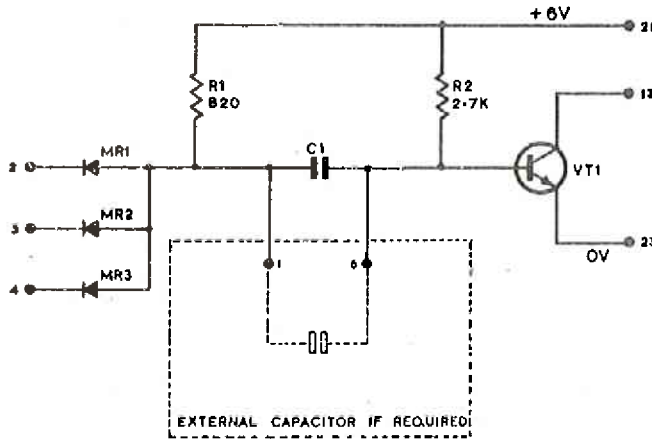
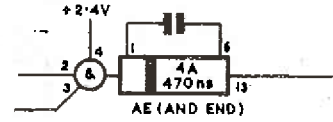
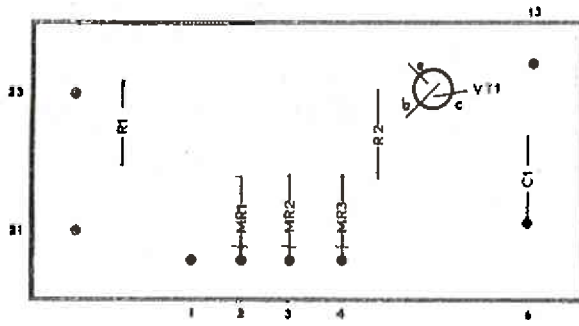
Alternative Layout.



VR (VOLTAGE REFERENCE)



TRANSISTOR VT1 PURCH. SPEC. PS 218 CAT. NO. 1100B



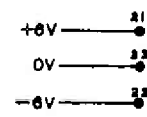
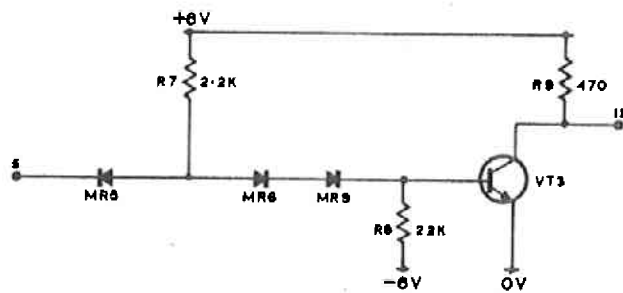
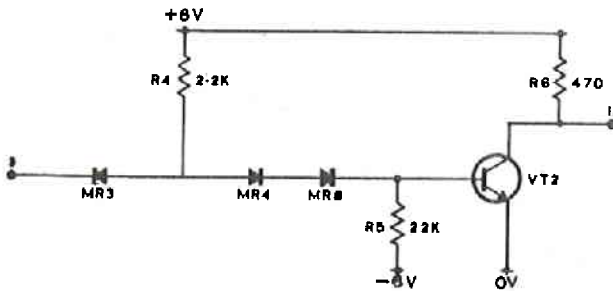
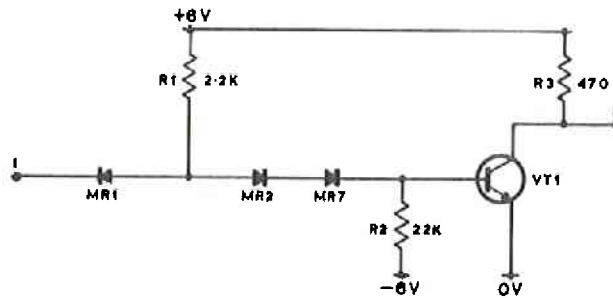
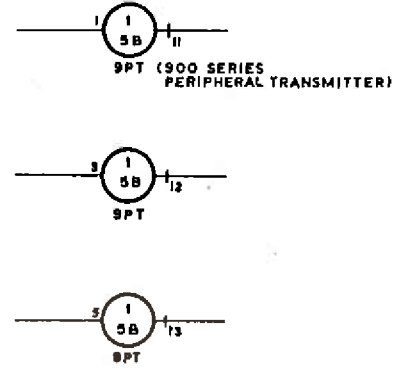
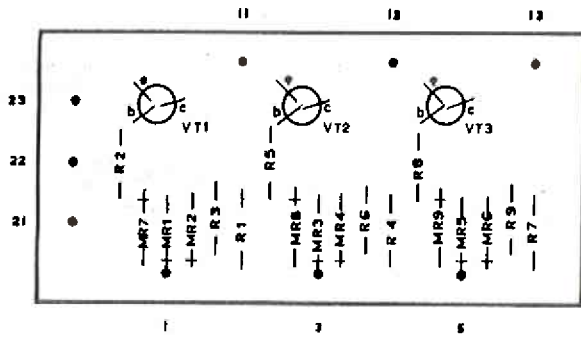
LSA N°	C1	PULSE WIDTH
09	470pF	470ns
14	680pF	680ns
130	22µF	220µs
131	2.2µF	2.2ms

NOTES:

- (1) OUTPUT PULSE POSITIVE
- (2) PULSE TRIGGERED BY ANY INPUT REVERTING TO '0' PROVIDING ALL I/P'S HAVE BEEN '1' FOR $>C/2ns$. (WHERE C = CAPACITANCE IN pF)
- (3) PULSE WIDTH = Cns (WHERE C = CAPACITANCE IN pF)
- (4) C1 MAY BE INCREASED BY EXTERNAL CAPACITOR

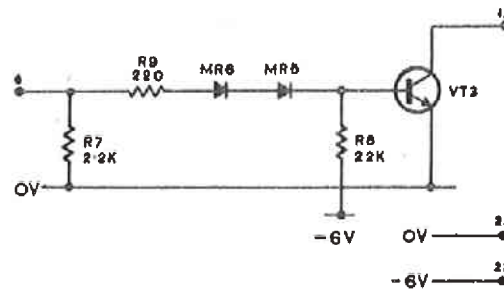
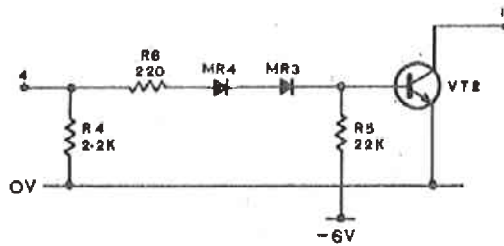
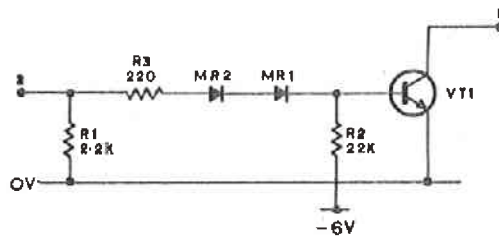
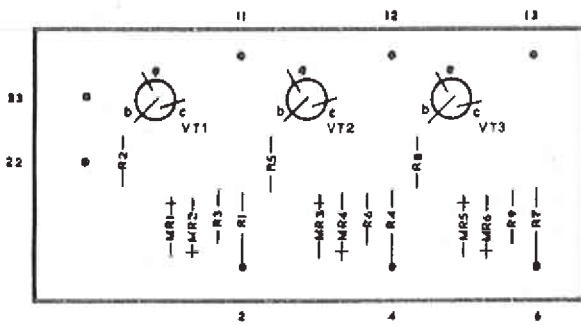
INPUT LOGIC LEVELS	
'1'	= > 2V
'0'	= < 1V

TRANSISTOR PURCH. SPEC. CAT. No.
VT1-VT3 PS 218 11008

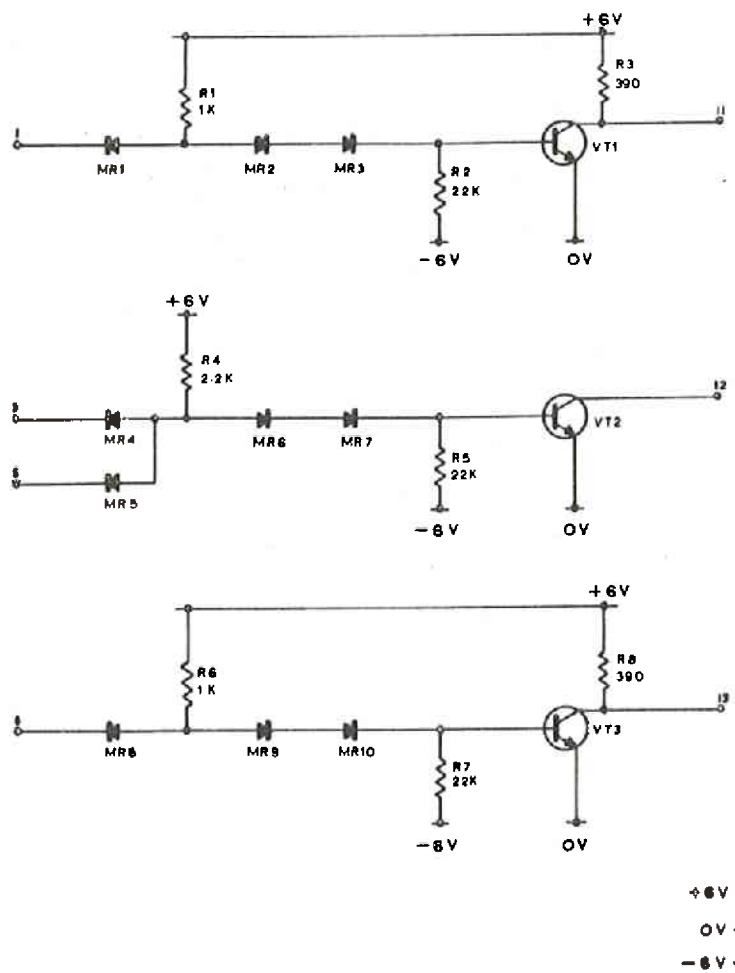
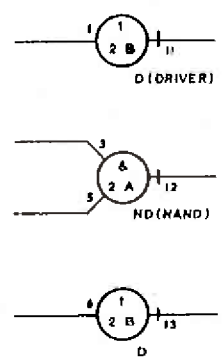
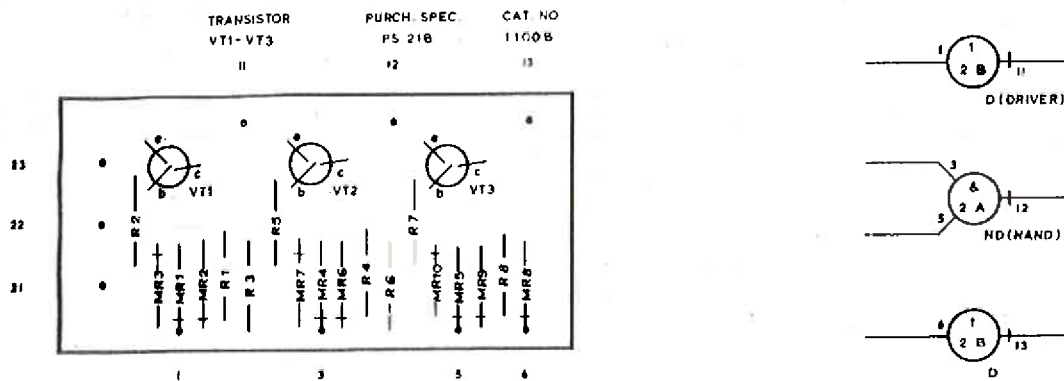


INPUT LOGIC LEVELS	
'1's	> 2V
'0's	< 1V

TRANSISTOR PURCH. SPEC. CAT. NO.
VT1-VT3 P5 218 11008

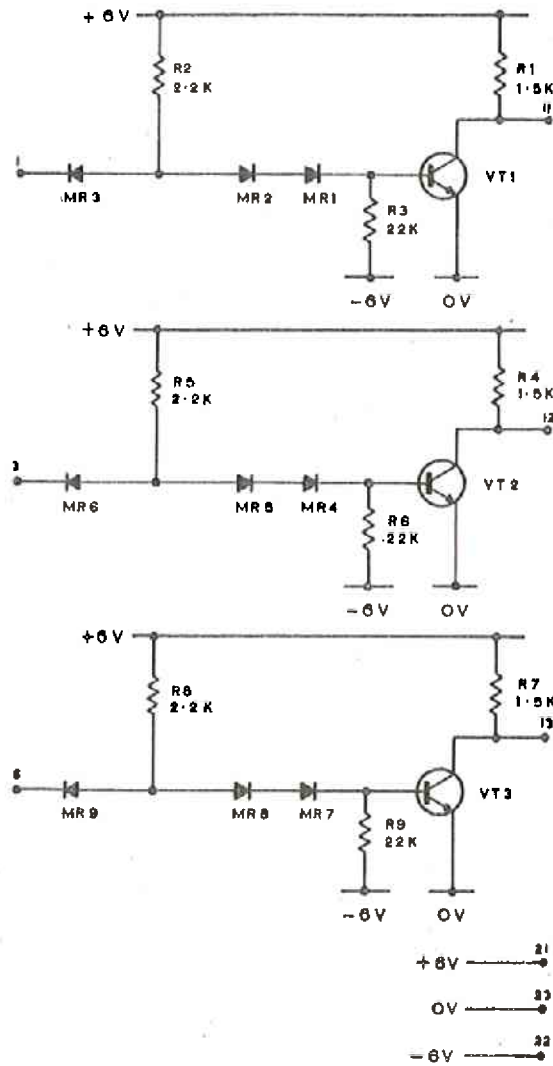
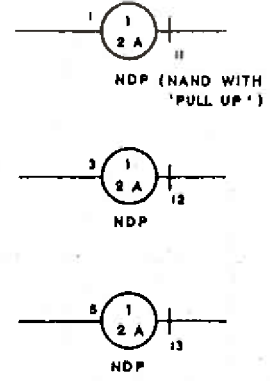
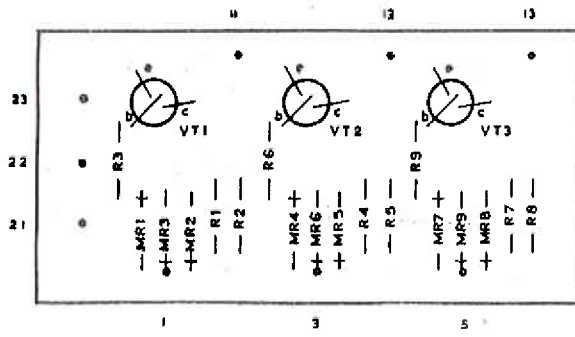


INPUT LOGIC LEVELS	
'1'	= > 3V
'0'	= < 1V



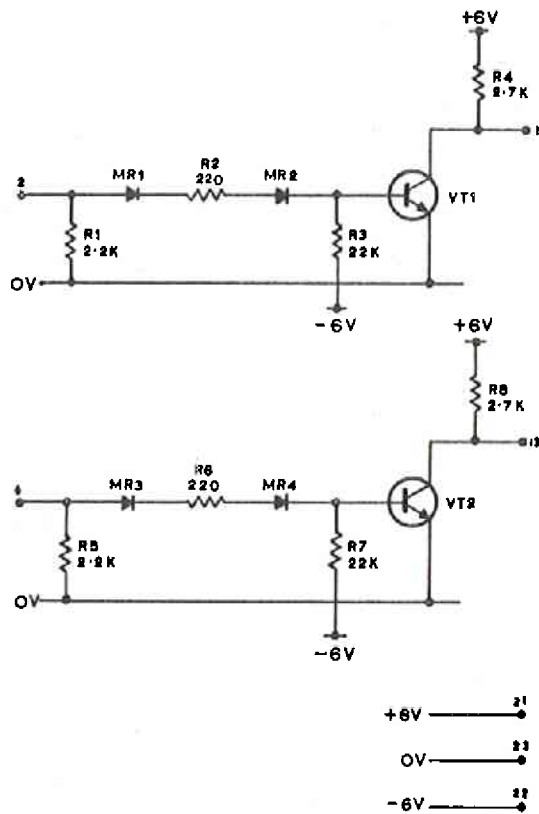
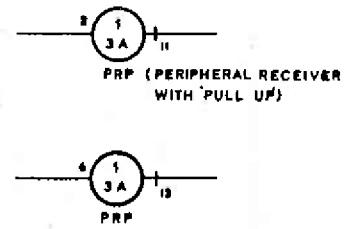
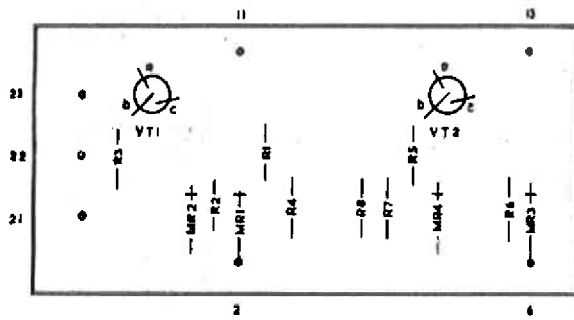
INPUT LOGIC LEVELS	
'1'	> 2V
'0'	< 1V

TRANSISTOR PURCH SPEC CAT NO.
VT1- VT3 PS 21B 1100B



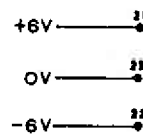
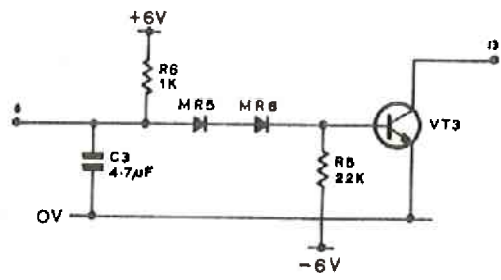
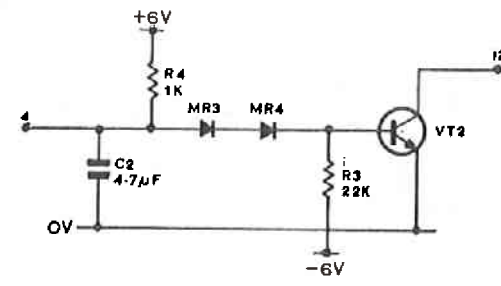
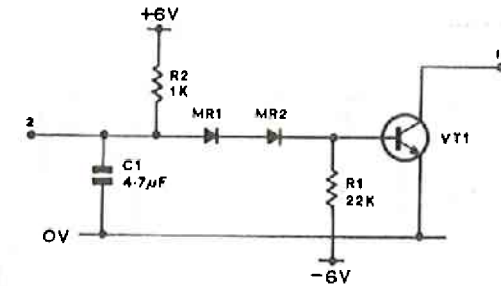
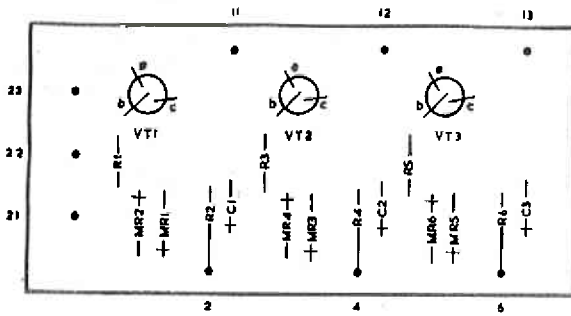
INPUT LOGIC LEVELS	
'1'	= > 2V
'0'	= < 1V

TRANSISTOR PURCH. SPEC. CAT. NO.
VT1, VT2 PS21B 1100B



INPUT LOGIC LEVELS	
'1'	$\geq 3V$
'0'	$\leq 1V$

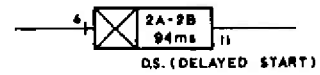
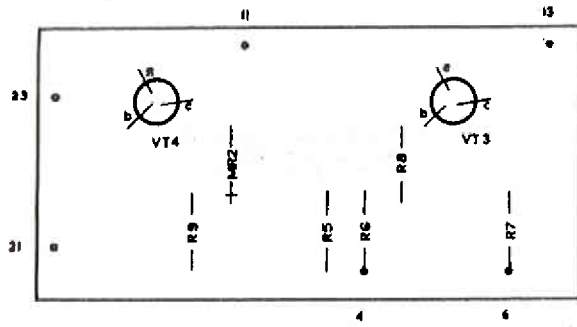
TRANSISTOR PURCH. SPEC. CAT. NO.
VT1-VT3 PS 218 11008



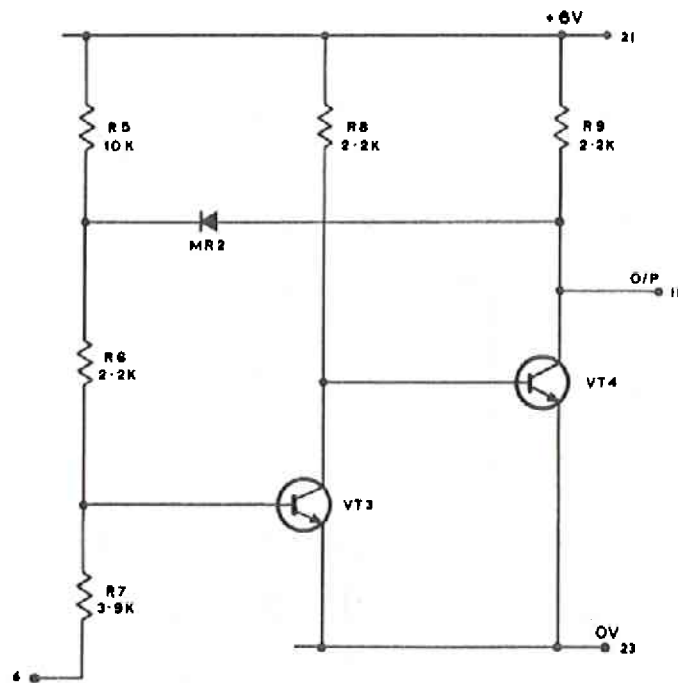
INPUT LOGIC LEVELS	
1	> 8V
0	< 1V

Figure 20 (ISSUE 2.)

TRANSISTOR PURCHASE SPEC. CAT. NO.
VT3 VT4 PS218 11008

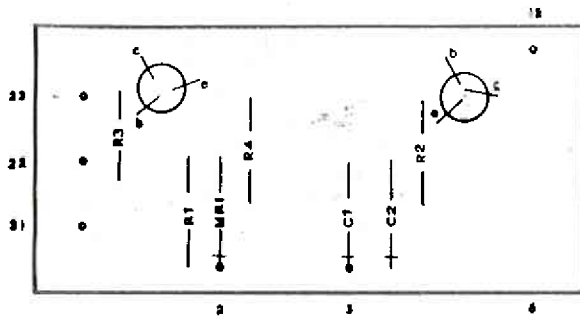


NOTE :-
L.S.A.19 ALWAYS FOLLOWS L.S.A.
20, 21, 24 OR 25. THE SYMBOL
SHOWN IS A COMBINED SYMBOL
FOR THE 2 ELEMENTS.

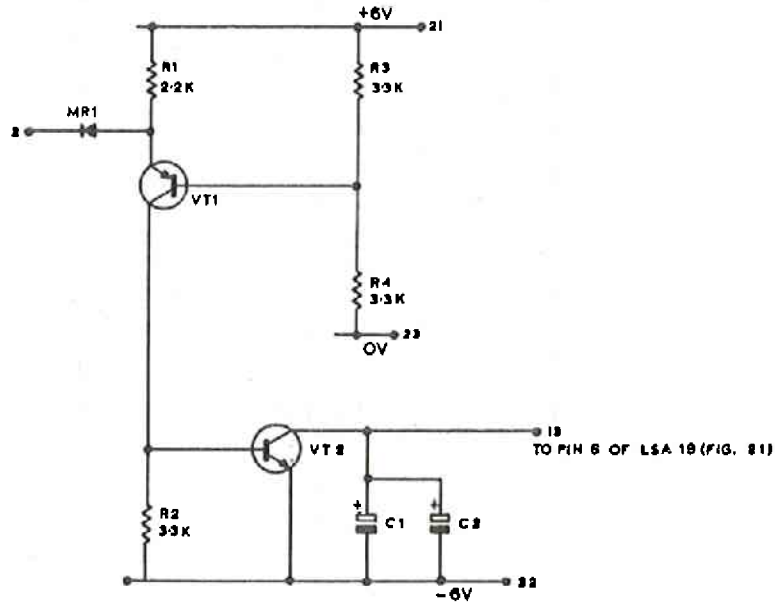


INPUT THRESHOLD LEVEL (AT 25°C) = 0.4V ±10%
--

TRANSISTOR	PURCH. SPEC.	CAT. NO.
VT1	-	14581
VT2	PS 218	11008



L.S.A. 19 ALWAYS FOLLOWS
L.S.A. 20, 24 OR 25
SEE FIG. 21 FOR COMBINED
SYMBOL.

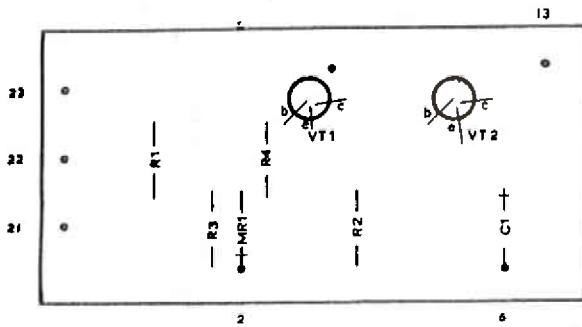


L.S.A. No.	C1 μ F	C2 μ F	DELAY ms
20	4.7	4.7	94
24	2.2	1.0	32
25	2.2	0.47	26.7

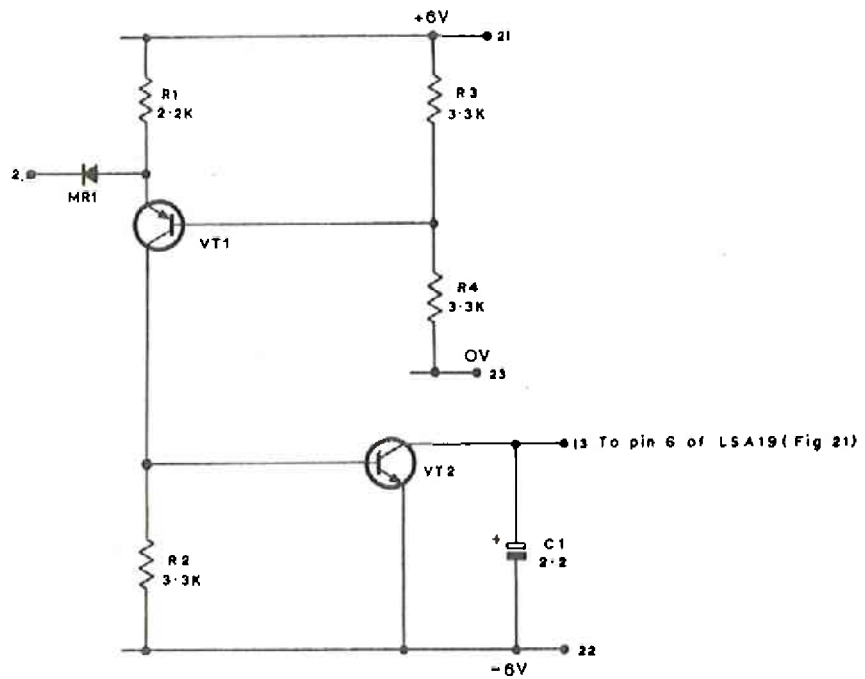
NOTE 1
DELAY Δ 10ms PER μ F (WHERE μ F IS CAPACITANCE OF C1 & C2)

INPUT LOGIC LEVELS
'1' = > 3V
'0' = < 1V

TRANSISTOR	PURCH. SPEC.	CAT. NO.
VT1	—	14561
VT2	PS 218	11008



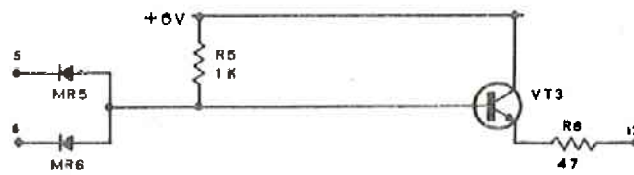
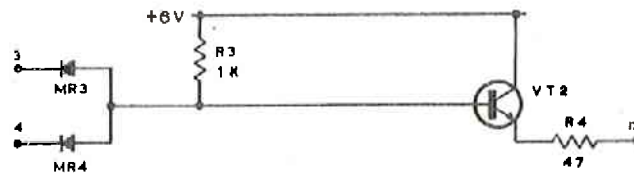
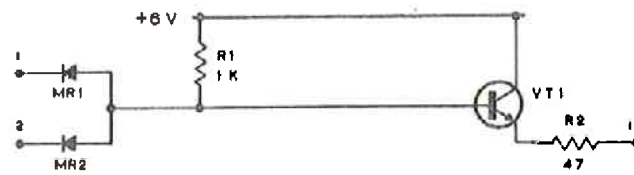
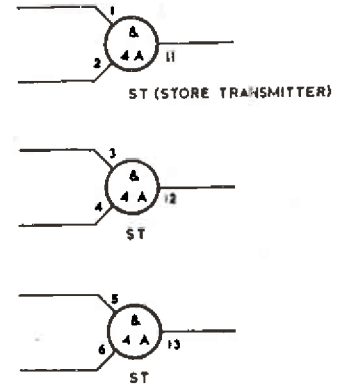
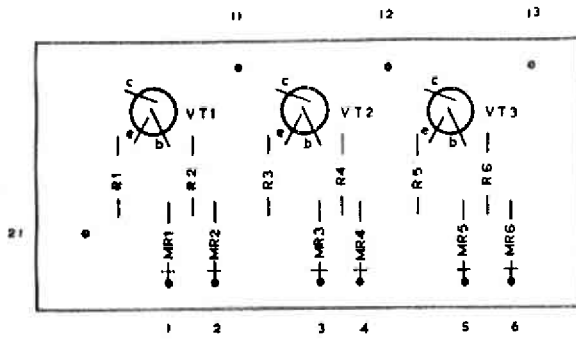
L.S.A. 19 ALWAYS FOLLOWS
L.S.A. 21 SEE FIGURE 21
FOR COMBINED SYMBOL.



NOTE:
1. DELAY Δ 10ms PER μ F
(WHERE μ F IS CAPACITANCE
OF C1) Δ 22ms.

INPUT LOGIC LEVELS	
'1'	\geq 3V
'0'	\leq 1V

TRANSISTOR	PURCH SPEC	CAT NO.
VT1 - VT3	PS 21B	1100B



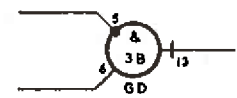
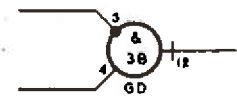
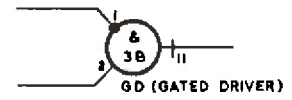
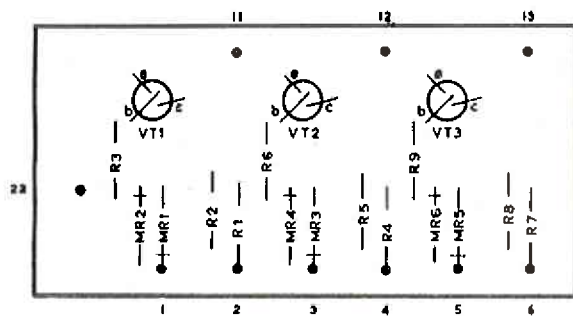
+6V ——— 21

INPUT LOGIC LEVELS	
(1)	O/P FOLLOWS I/P OVER RANGE 0V TO 4.7V
(2)	WHEN DRIVING A RECEIVER THE LOGIC LEVELS ARE :-
'1'	= > 3V
'0'	= < 1V

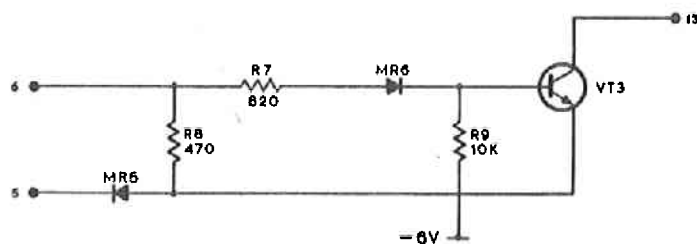
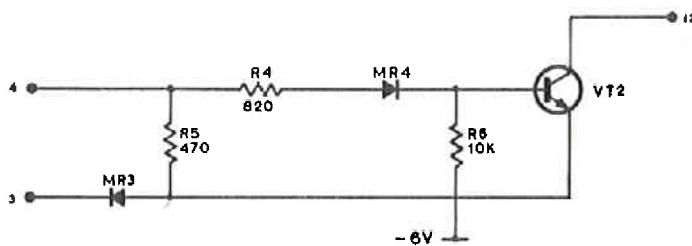
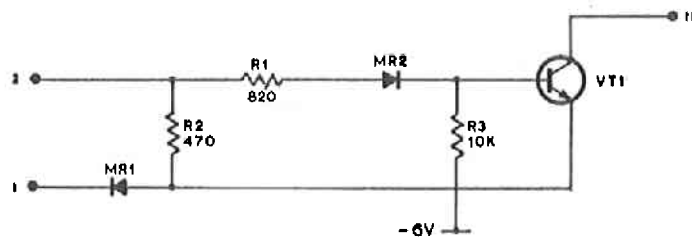
TRANSISTOR
VT1 - VT3

PURCH. SPEC.
P5 218

CAT. NO.
11008

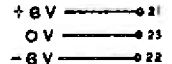
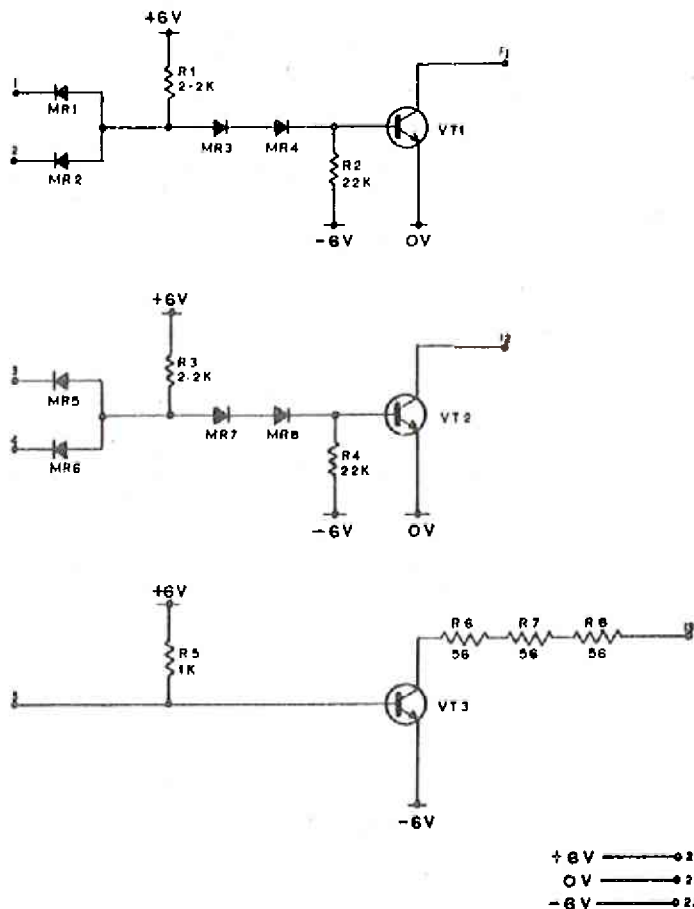
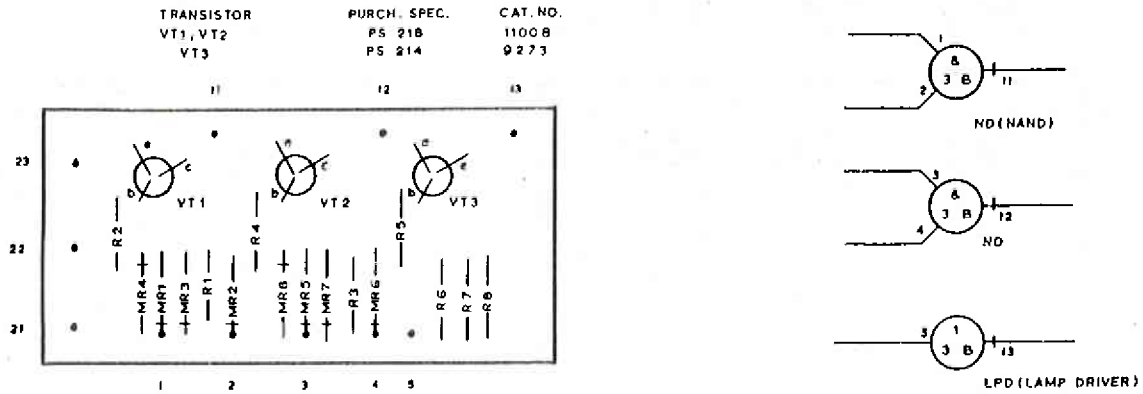


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SEE
ERRATA
PAGE 1



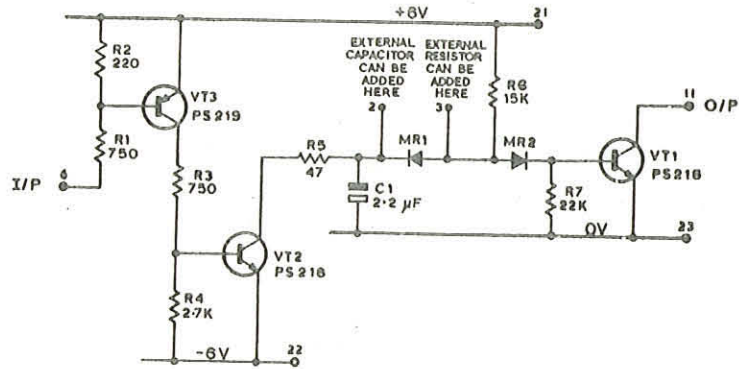
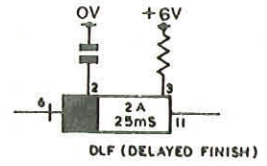
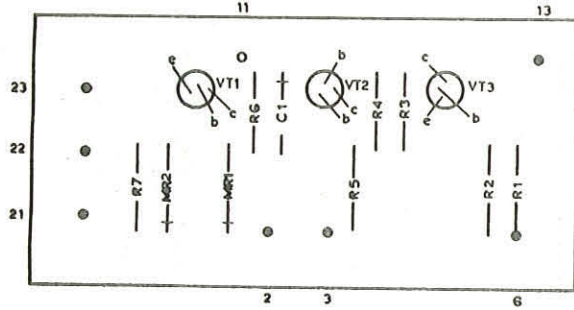
-6V

INPUT LOGIC LEVELS	
'1'	> 3V
'0'	< 1V

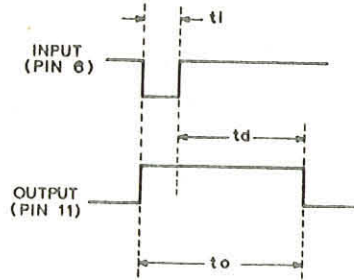


INPUT LOGIC LEVELS	
NAND	'1' = > 2 V
GATES	'0' = < 1 V
LAMP DRIVER	'1' = > 0.45 V
DRIVER	'0' = < 0.25 V

TRANSISTOR	PURCH. SPEC.	CAT. No.
VT1, VT2	PS 218	11008
VT3	PS 219	11009



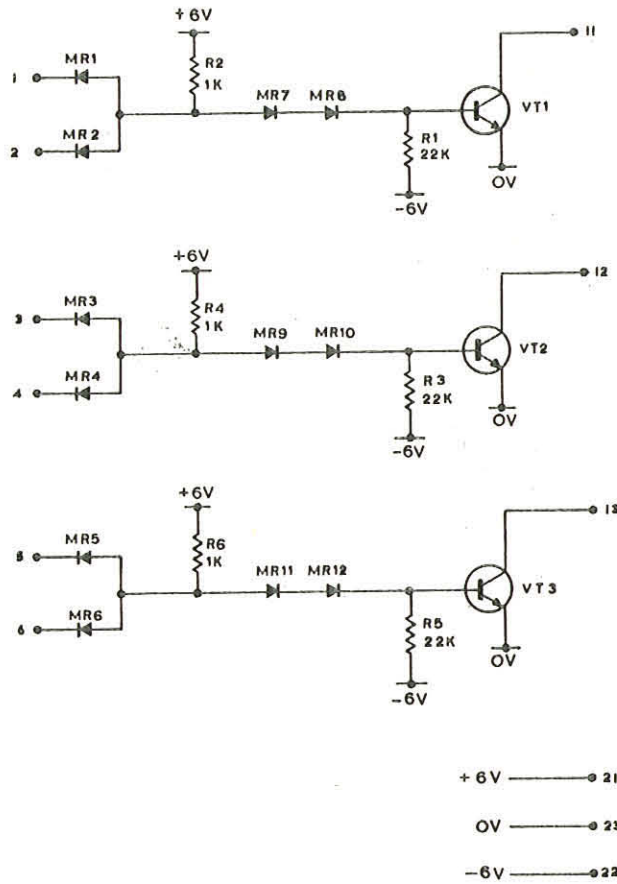
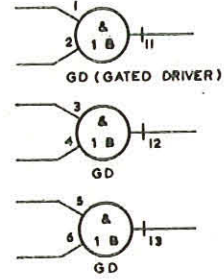
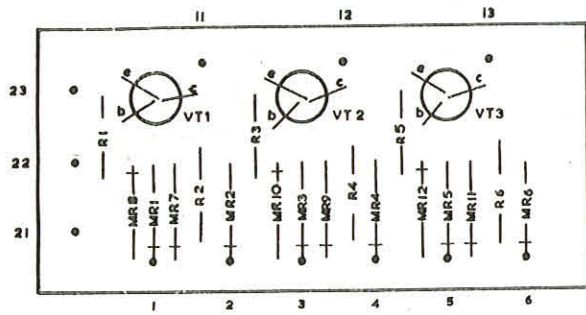
- NOTE:
1. SHUNT C1 TO MAKE O/P > 25mS.
 2. SHUNT R6 TO MAKE O/P < 25mS.



td NOMINAL = 25mS
td RANGE = 1m - 5 Secs.
td TOLERANCE = ± 30%

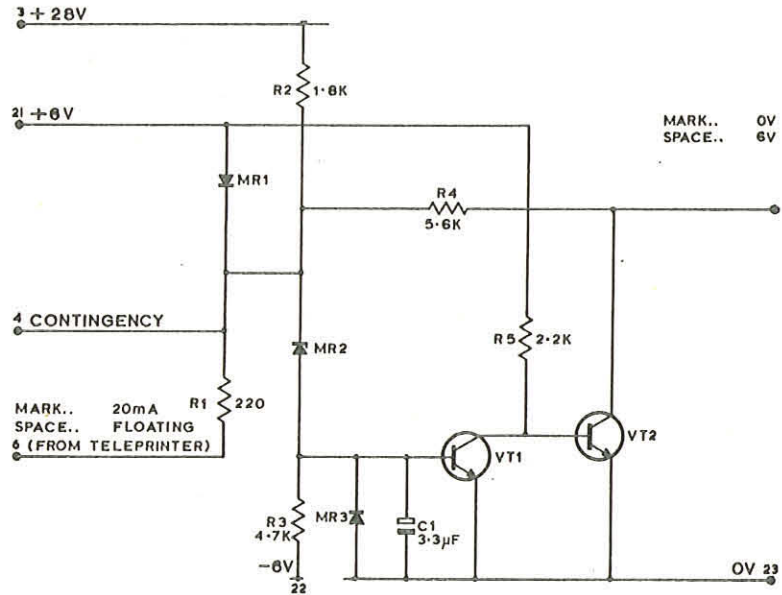
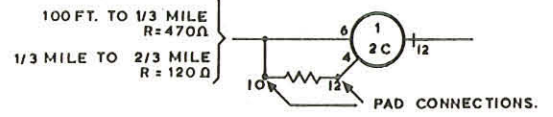
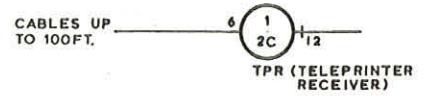
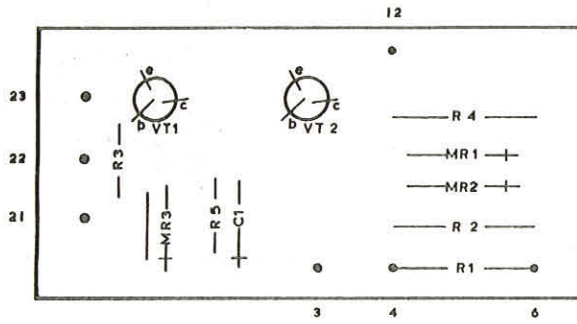
INPUT LOGIC LEVELS	
'1'	= > 5.4V
'0'	= < 1V

TRANSISTOR PURCH SPEC. CAT. NO.
VT1 - VT3 P 5 21B 1100B



INPUT LOGIC LEVELS	
'1'	> 2V
'0'	< 1V

TRANSISTOR PURCH. SPEC. CAT. No.
VT1, VT2 PS 218 11008

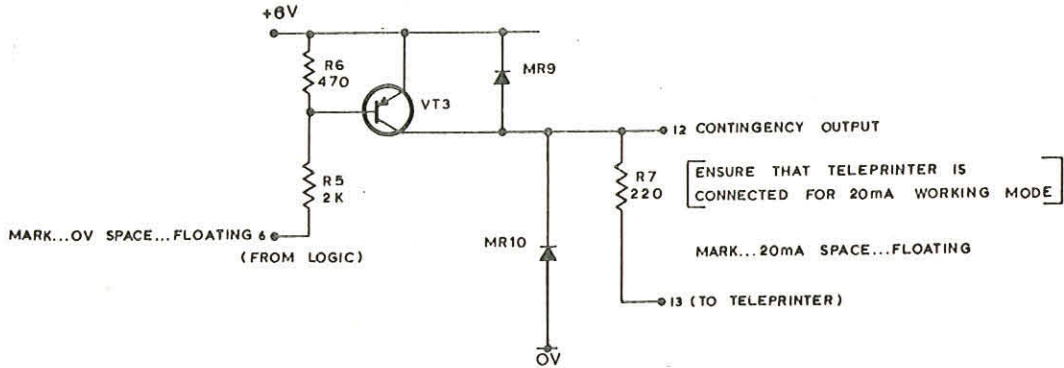
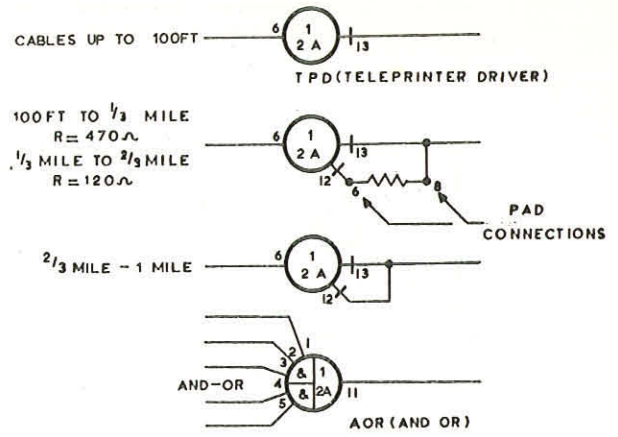
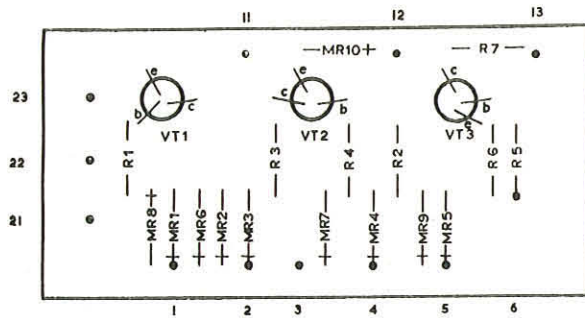


NOTE:
THE ELEMENT IS CONSIDERED TO INVERT BECAUSE THE MARK CURRENT IS TAKEN TO REPRESENT A LOGIC "1", EVEN THOUGH THE POTENTIAL AT PIN 6 FALLS UNDER MARK CONDITIONS.

INPUT LOGIC LEVELS	
0	> 5V
1	< 0.4V (ASSUMING NO EXTERNAL R AT PIN 4)

4100/900
4.6.1.

TRANSISTOR PURCH. SPEC. CAT. NO.
VT1, VT2 PS 21B 1100B
VT3 PS 219 11009



TELEPRINTER DRIVER

INPUT LOGIC LEVELS	
'1'	= > 4V
'0'	= < 1V

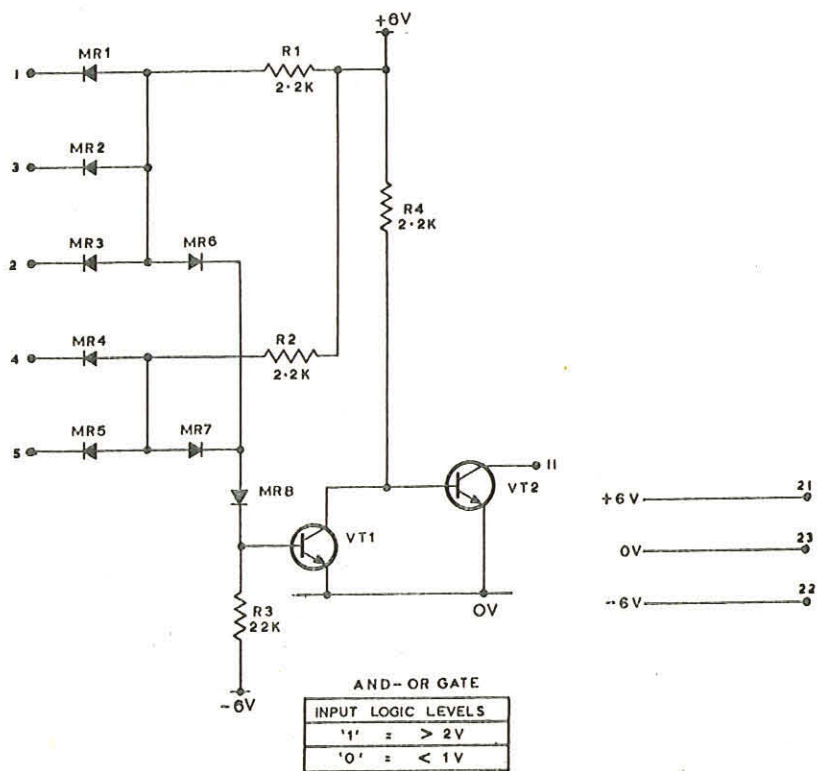
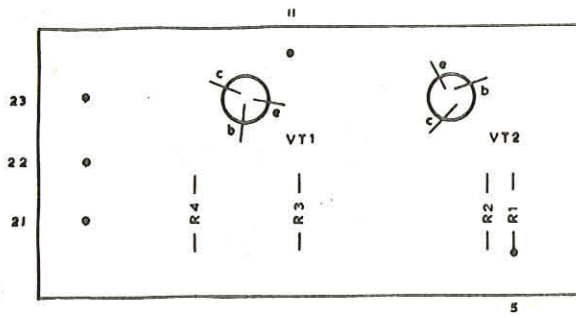
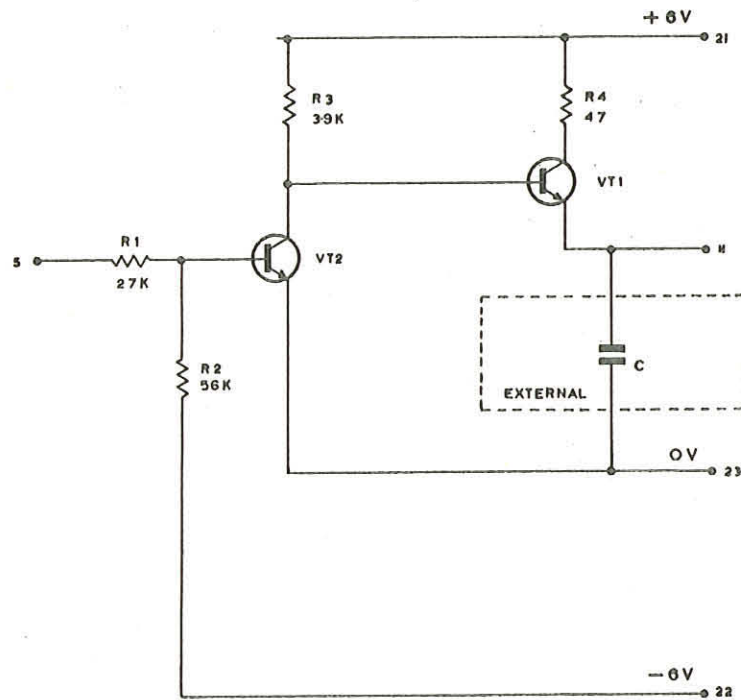


Figure 30 (ISSUE 2)

TRANSISTOR	PURCH SPEC	CAT NO.
VT1, VT2	PS 212	88 43



SEE FIGURE 32 FOR SYMBOL



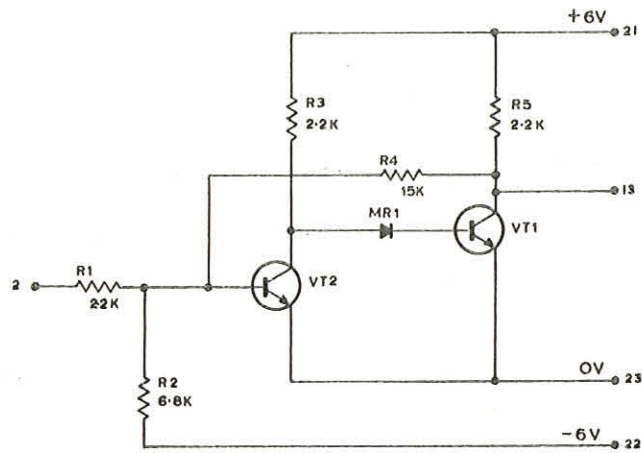
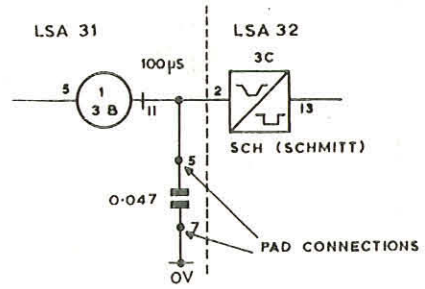
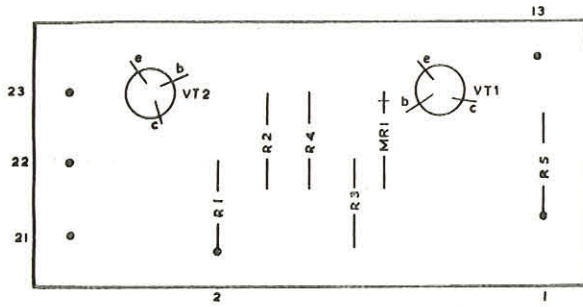
NOTES:

- (1) INPUT VOLTAGE LEVELS ARE '1' = $+12V \pm 3V$; '0' = $0V \pm 3V$
- (2) C. IS CONNECTED EXTERNALLY WHEN USED IN CONJUNCTION WITH A RESISTOR ON LSA 32
- (3) C. = $0.047 \mu F$ FOR A DELAY OF $100 \mu S$.

TRANSISTOR
VT1, VT2

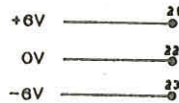
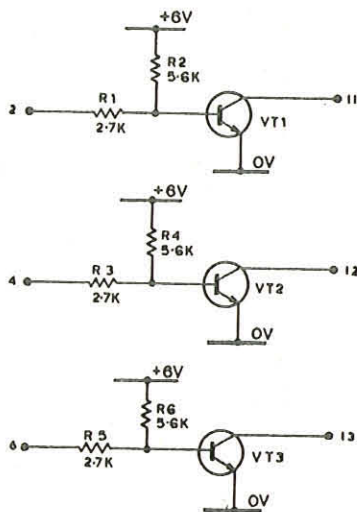
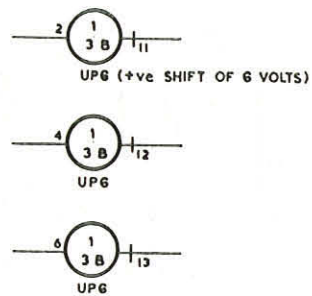
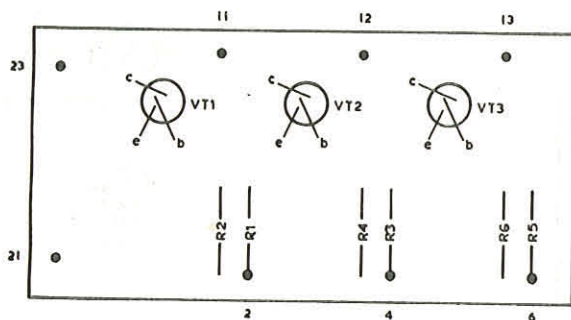
PURCH. SPEC.
PS 212

CAT. NO.
8843



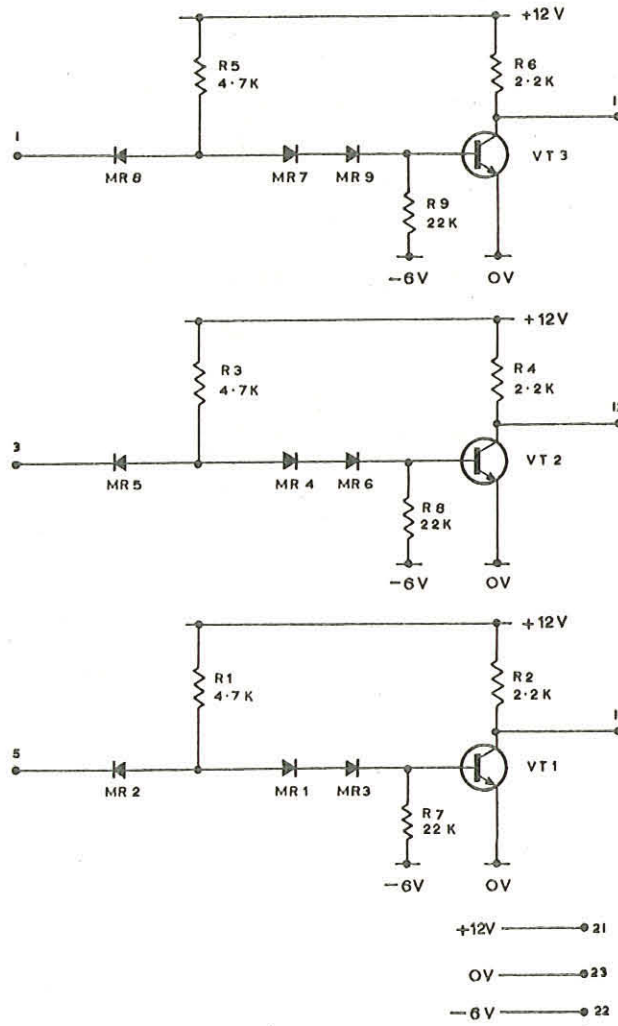
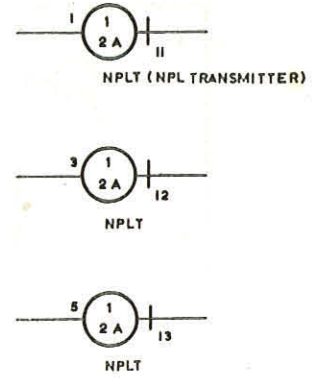
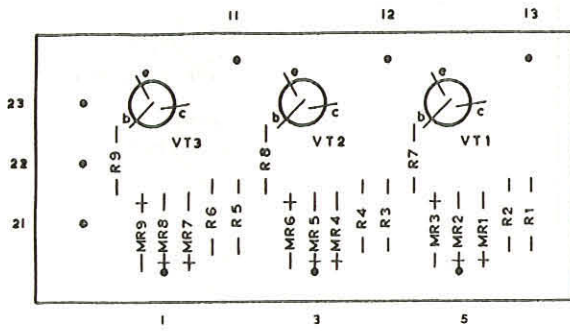
THRESHOLD VOLTAGE AT PIN 2	OUTPUT WAVEFORM PIN 13
RISING VOLTAGE +3.1V	
FALLING VOLTAGE +2.4V	

TRANSISTOR PURCH. SPEC. CAT. No.
VT1-VT3 PS 21B 1100B



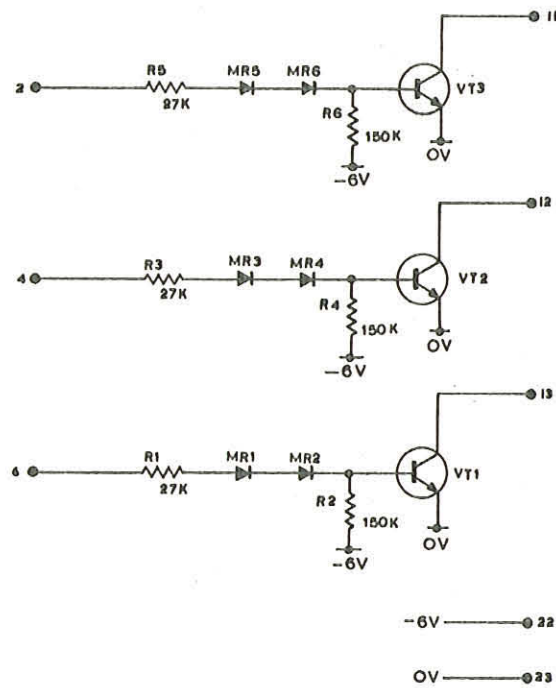
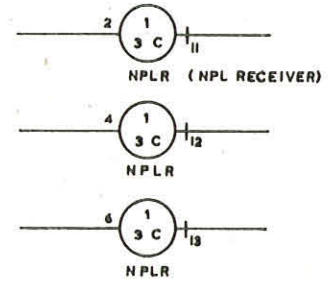
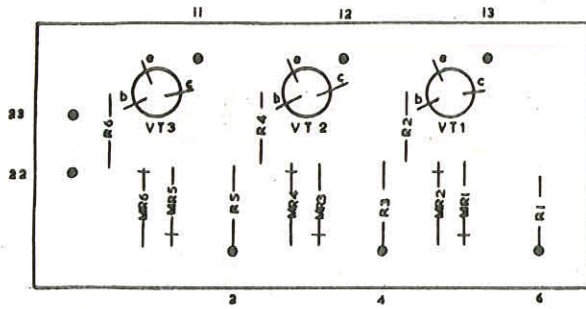
INPUT LOGIC LEVELS	
'1'	= > -1.2V
'0'	= < -3V

TRANSISTOR	PURCH SPEC	CAT NO.
VT1-VT3	PS 218	11008

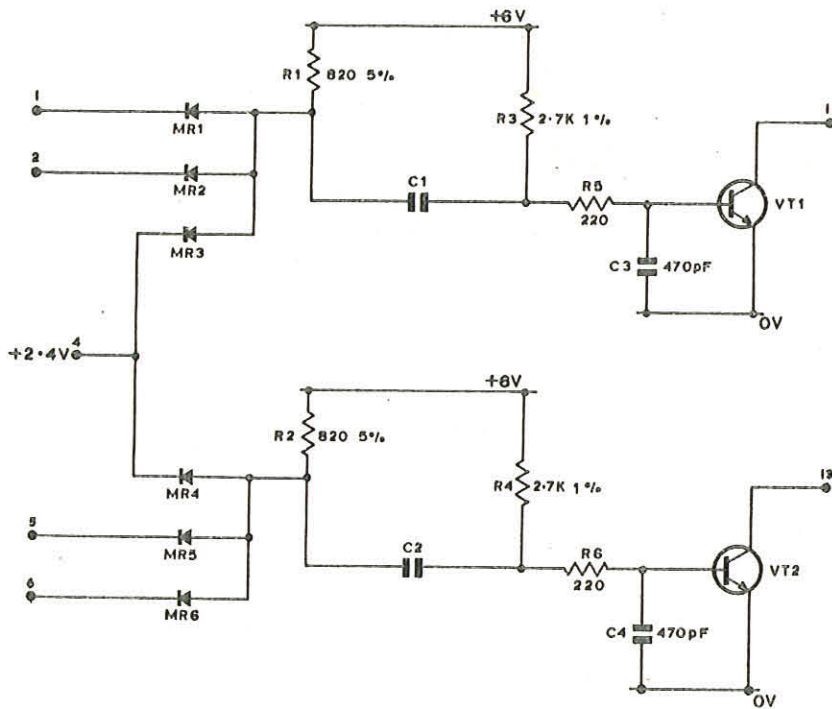
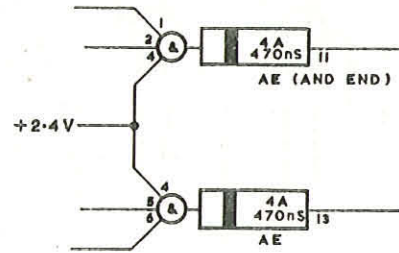
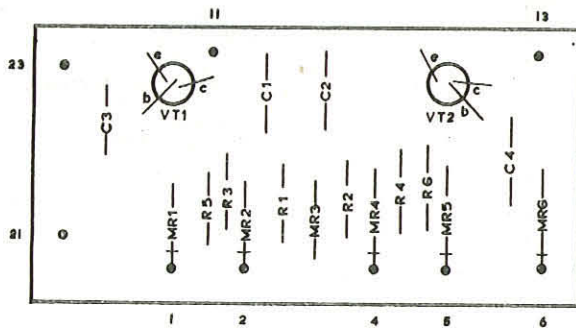


INPUT LOGIC LEVELS	
'1'	= > 2
'0'	= < 1

TRANSISTOR **PURCH. SPEC.** **CAT. NO.**
VT1 - VT3 PS 218 11008



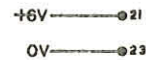
INPUT LOGIC LEVELS	
"1"	> 2
"0"	< 1



PULSE WIDTH = $C_n S$ (WHERE C = CAPACITANCE IN pF.)

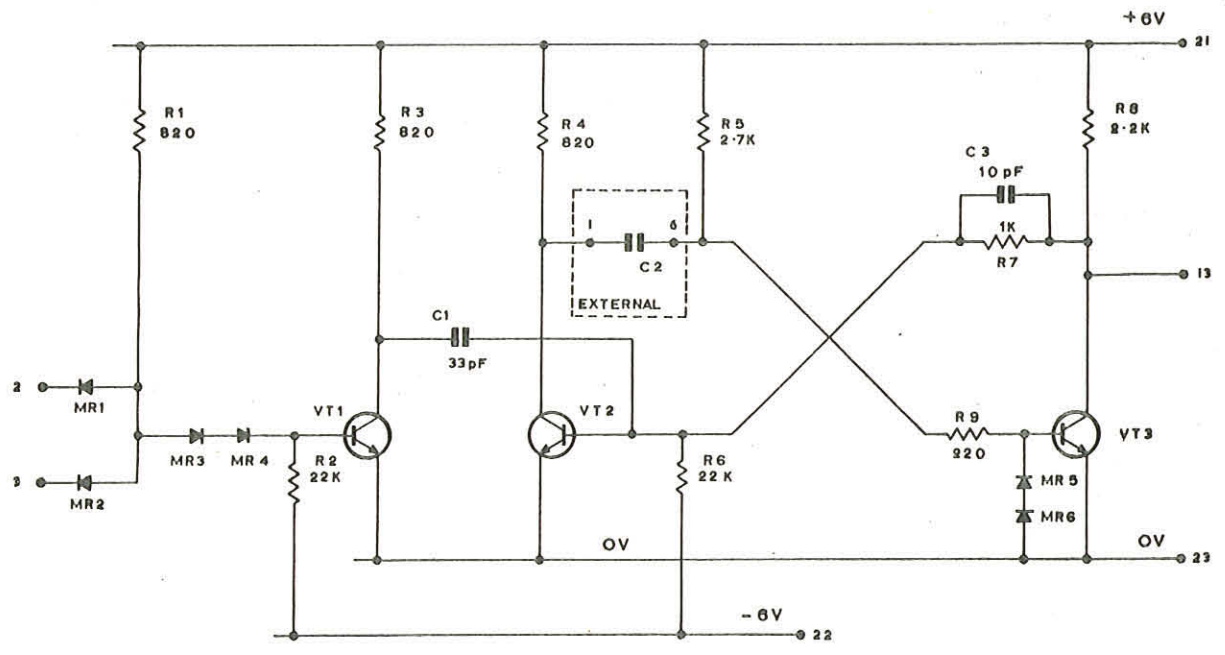
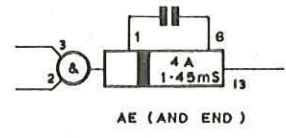
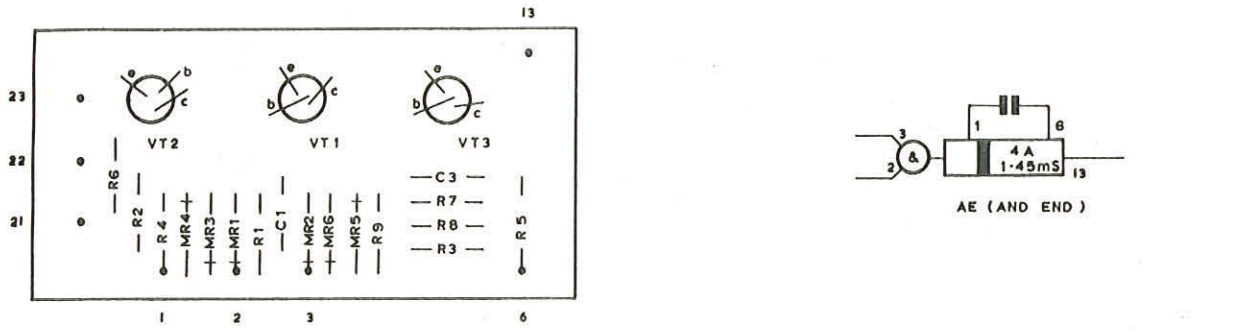
	UPPER ELEMENT	LOWER ELEMENT
L.S.A.	C1	C2
37	680pF	680pF
39	100pF	100pF
40	330pF	330pF
41	220pF	220pF
42	470pF	470pF

- NOTES:
- (1) OUTPUT PULSE POSITIVE.
 - (2) PULSE TRIGGERED BY ANY INPUT REVERTING TO '0' PROVIDED ALL I/P'S HAVE BEEN '1' FOR GREATER THAN $C/2$ ns. (WHERE C = CAPACITANCE IN pF.)



INPUT LOGIC LEVELS
↑ = > 2.4V
↘ = < 1V

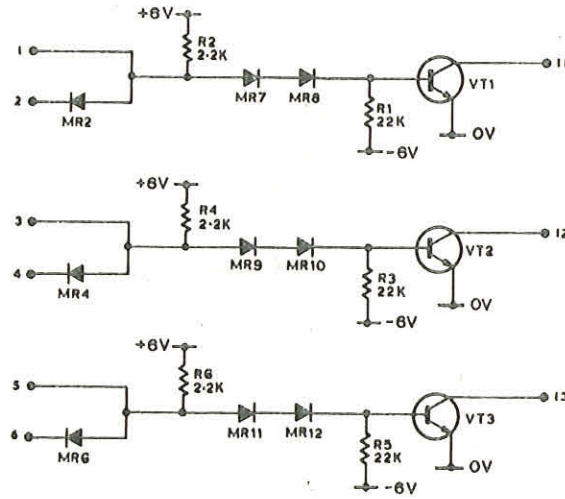
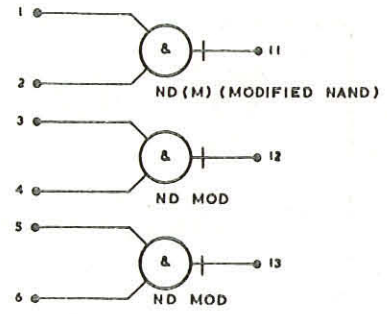
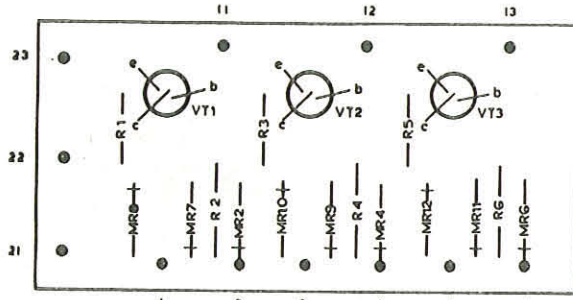
TRANSISTOR PURCH. SPEC CAT NO.
VT1-VT3 PS 218 11008



- NOTES:
- (1) C2 IS EXTERNAL AND SETS PULSE WIDTH
 - (2) OUTPUT PULSE POSITIVE
 - (3) PULSE TRIGGERED BY ANY INPUT REVERTING TO A '0' PROVIDED OTHER INPUT IS A '1'
 - (4) PULSE WIDTH $T = 1.36 \times C2 \text{ nS} \pm 36\%$
(WHERE C2 IS IN pF)

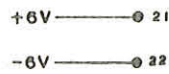
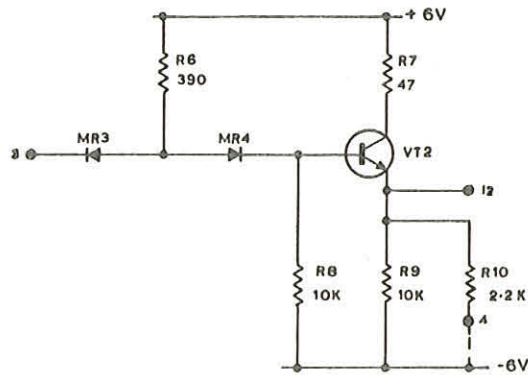
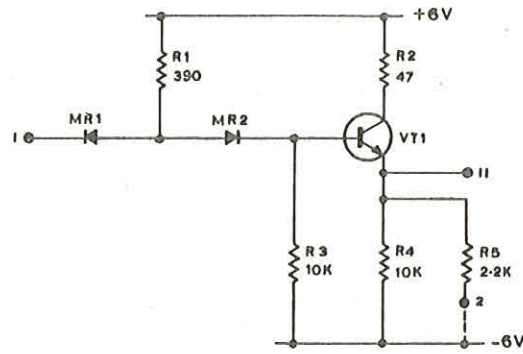
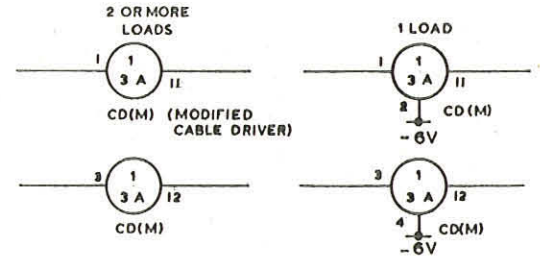
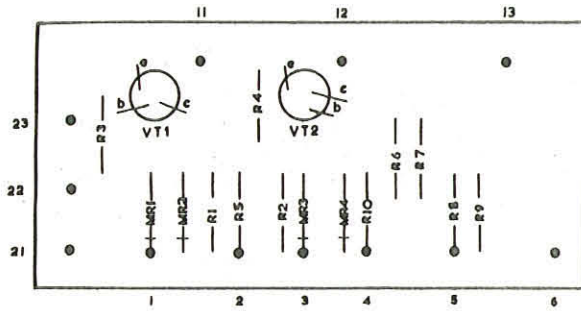
INPUT LOGIC LEVELS	
'1'	> 2
'0'	< 1

TRANSISTOR PURCH. SPEC. CAT. No.
VT1-VT3 PS 21B 1100B

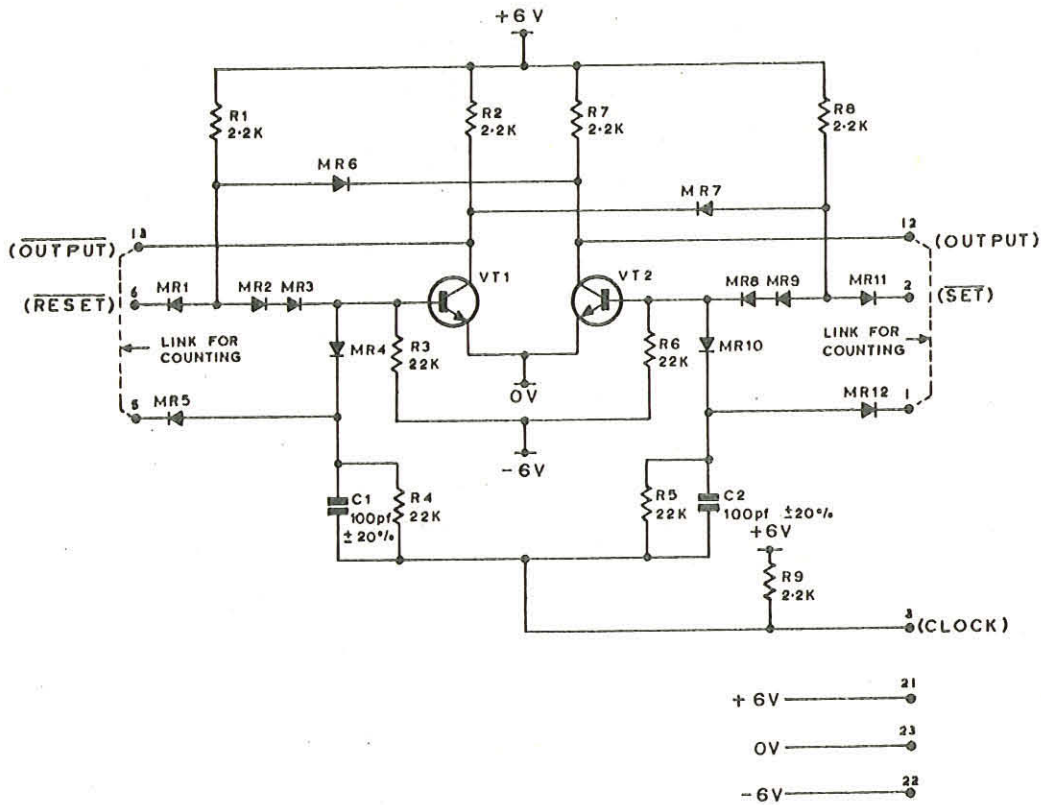
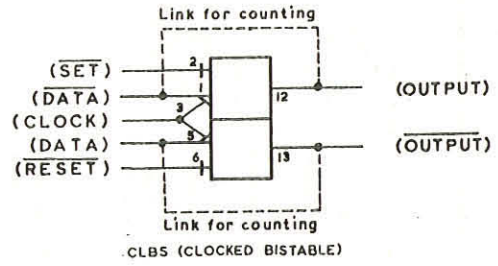
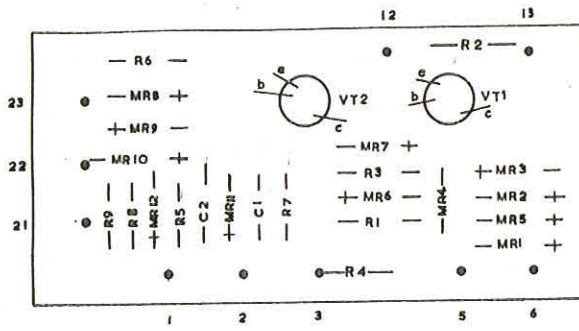


INPUT LOGIC LEVEL	
'1'	= > 2V
'0'	= < 1V

TRANSISTOR PURCH. SPEC. CAT. NO.
VT1 VT2 P5 216 11008

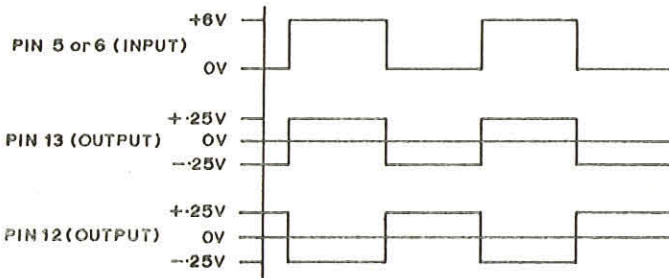
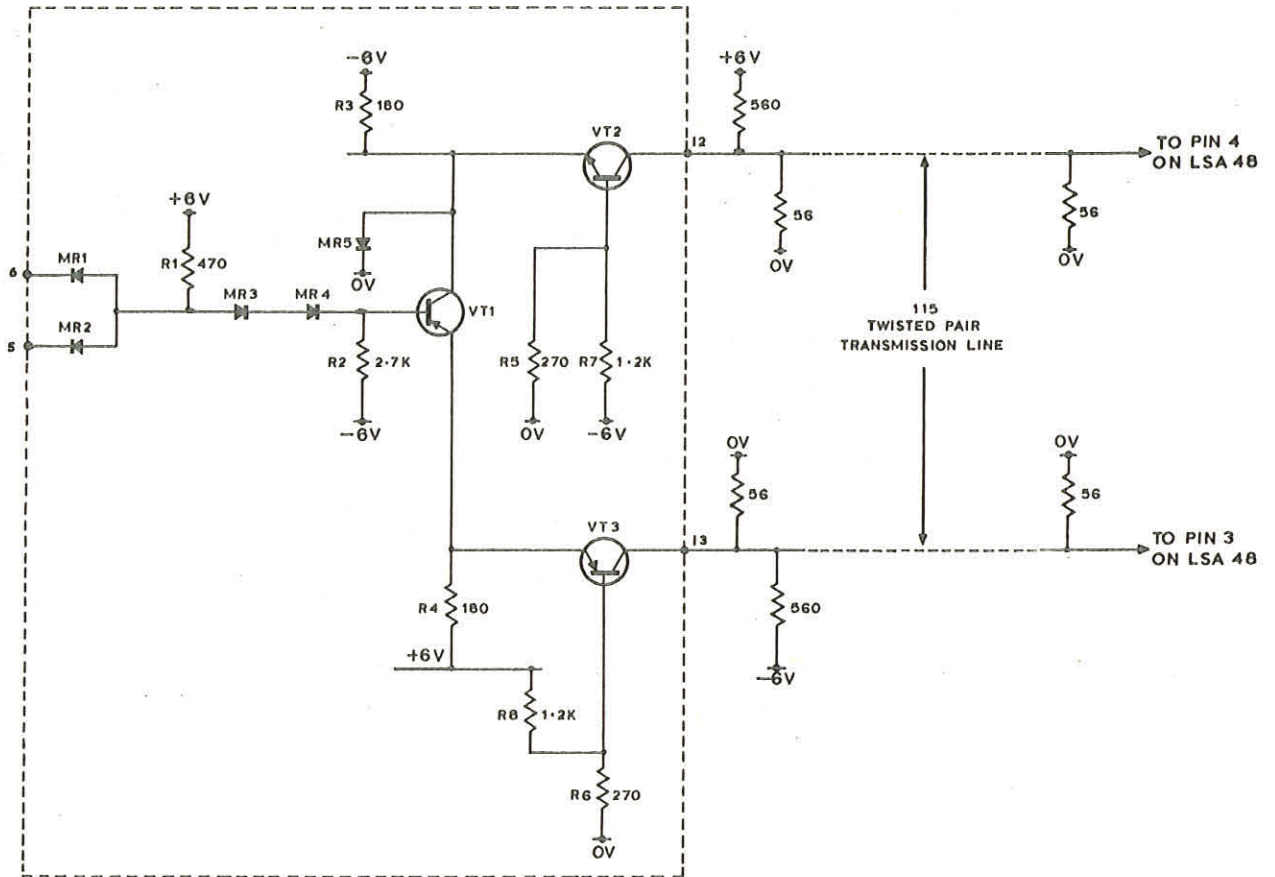
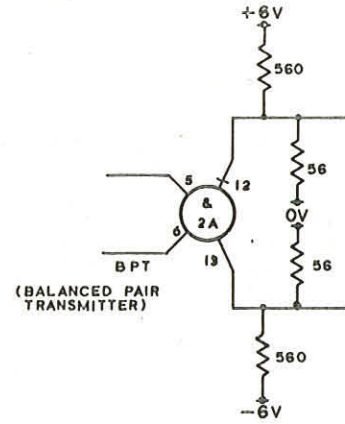
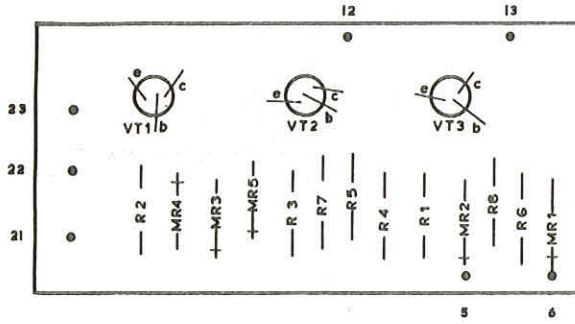


INPUT LOGIC LEVELS	
'1'	= > 2V
'0'	= < 1V



INPUT LOGIC LEVELS	
'1'	> 2 V
'0'	< 1 V

TRANSISTOR	PURCH SPEC.	CAT. No.
VT1, VT3.	PS 216.	9725.
VT2.	PS 212.	8843.



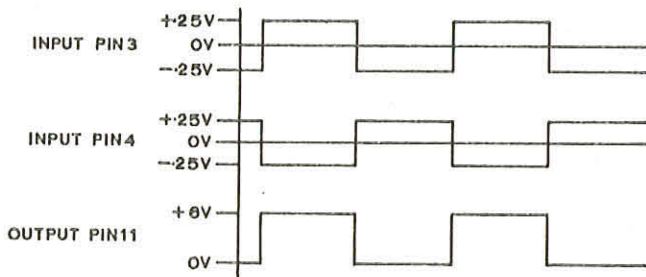
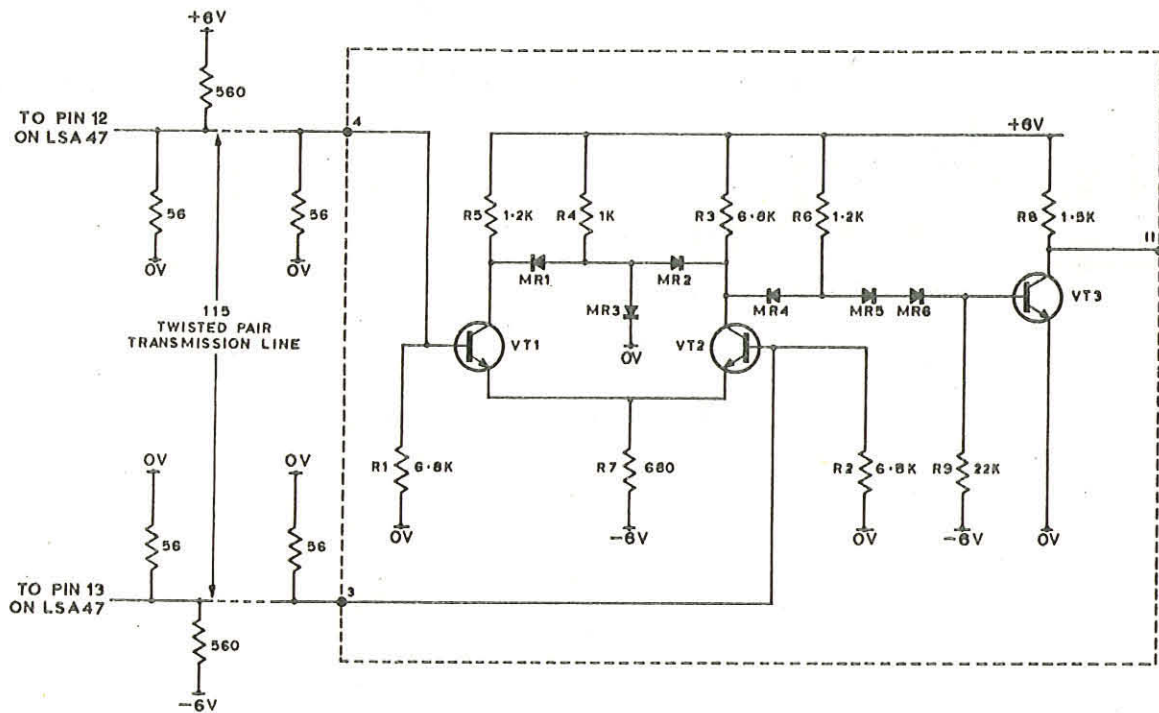
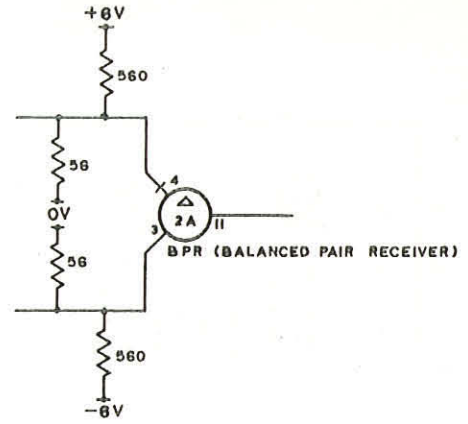
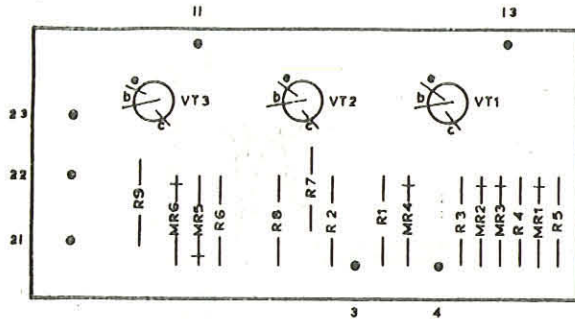
+6V — 21
0V — 23
-6V — 22

NOTE:
THE OUTPUT WAVEFORMS ABOVE ARE THOSE OBTAINED WITH TERMINATION AND BIASING AS USED ON THE CDC INTERFACE. THE 56Ω TERMINATING RESISTORS MUST BE ON EACH END OF THE TRANSMISSION LINE. THE 560Ω BIASING RESISTORS MAY BE AT EITHER END OF THE LINE, BUT NOT AT BOTH.

INPUT LOGIC LEVELS
↑ = > 2V
↓ = < 1V

4100/900.
4.6.1.

TRANSISTOR	PURCH. SPEC.	CAT No.
VT1, VT2	PS 212	8843
VT3	PS 218	11008



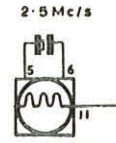
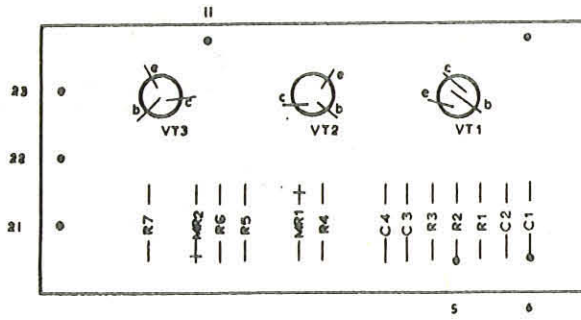
+6V — 21
0V — 23
-6V — 22

NOTE:
THE INPUT WAVEFORMS ABOVE ARE THOSE OBTAINED WITH TERMINATION AND BIASING AS USED ON THE CDC INTERFACE. THE 56Ω TERMINATING RESISTORS MUST BE ON EACH END OF THE TRANSMISSION LINE. THE 560Ω BIASING RESISTORS MAY BE AT EITHER END OF THE LINE, BUT NOT AT BOTH.

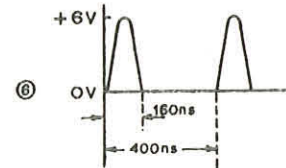
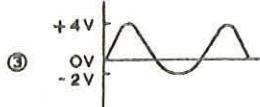
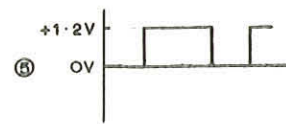
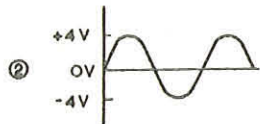
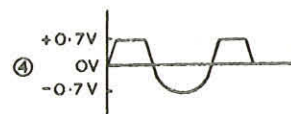
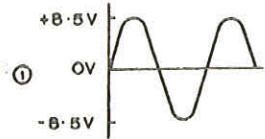
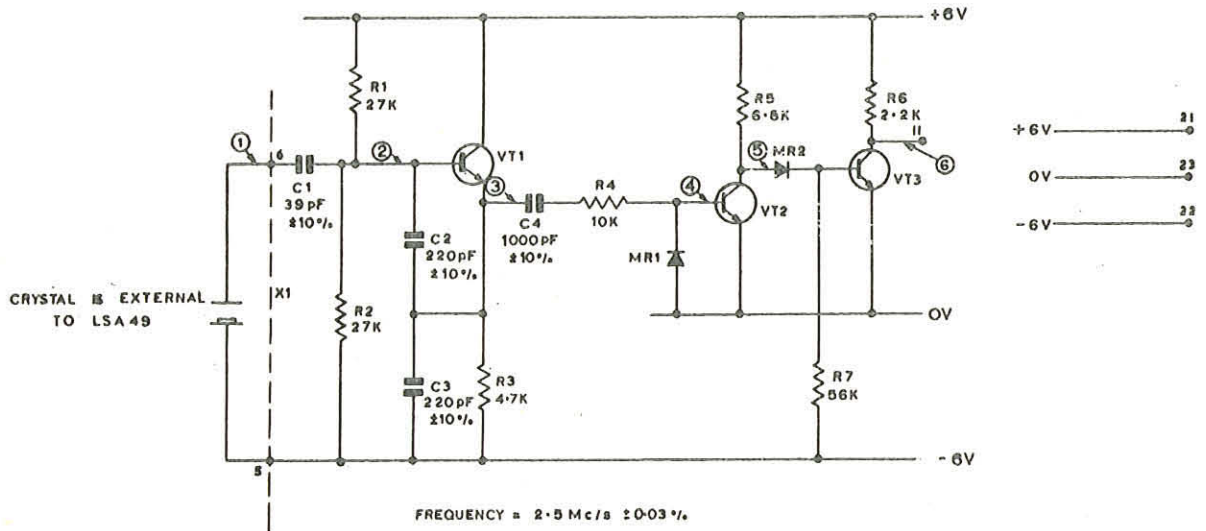
INPUT LOGIC LEVELS	
1	= PIN 4 > PIN 3 BY 0.4V MIN. 0.6V MAX.
0	= PIN 3 > PIN 4 BY 0.4V MIN. 0.6V MAX.

Figure 42. (ISSUE 2)

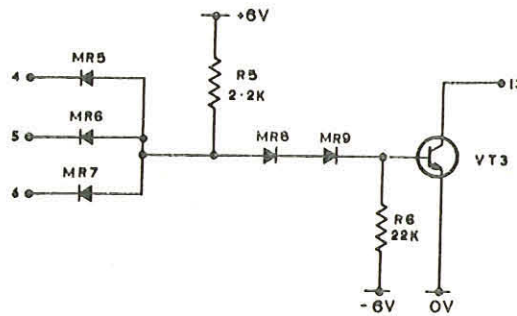
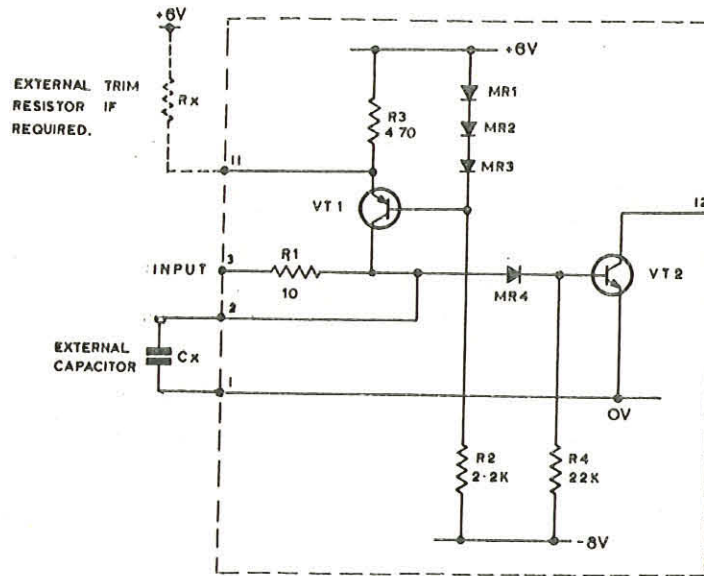
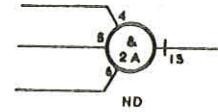
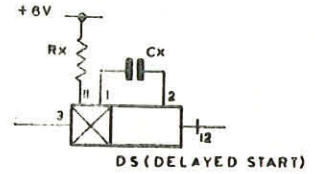
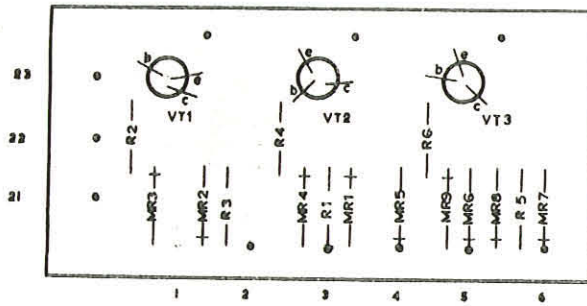
TRANSISTOR	PURCH. SPEC.	CAT. NO.
VT1	—	13053
VT2 VT3	PS218	11008



CO (CRYSTAL OSCILLATOR)



TRANSISTOR	PURCH. SPEC.	CAT. NO.
VT1	PS 219	11009
VT2,VT3	PS 210	11008



ADD:
 $TR \approx 35 + 0.44 C_x \text{ ns}$
 (where C_x is in pF)
 $TF \approx 30 + 0.05 TR \text{ ns}$
 (where TR is in ns)



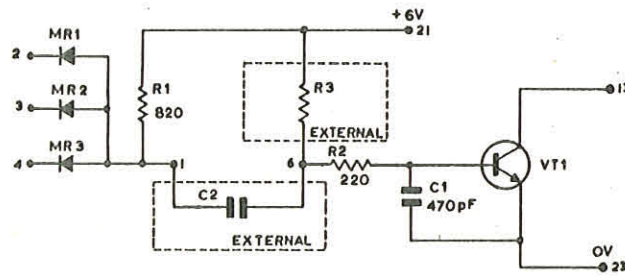
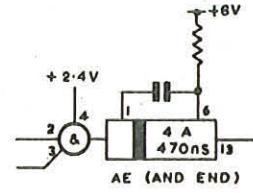
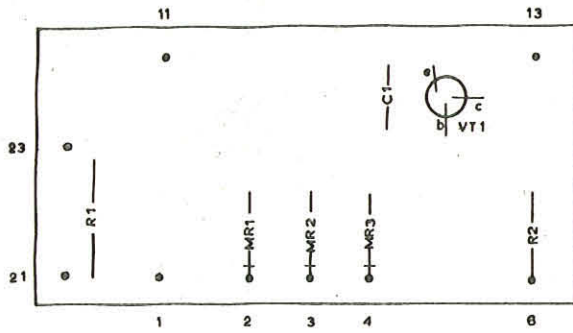
NOTE:
 1. Assuming connection to driving source is not more than 6ins long.

INPUT LOGIC LEVELS	
DELAY	'1's > 0.25V AT 3mA
ELEMENT	'0's = OPEN CIRCUIT
NAND	'1's > 2V
GATE	'0's < 1V

Value	Tol.	Voltage	Cat. No.	Nominal Delay
220 pf	$\pm 5\%$	400V	9313	132 \pm 32.9 ns.
330 pf	$\pm 5\%$	400V	8479	180 \pm 45.1 ns.
470 pf	$\pm 5\%$	400V	7916	242 \pm 60.4 ns.
680 pf	$\pm 5\%$	400V	8480	334 \pm 83.6 ns.
1000 pf	$\pm 5\%$	400V	7917	475 \pm 119 ns.
1500 pf	$\pm 5\%$	400V	7924	695 \pm 174 ns.
2200 pf	$\pm 5\%$	400V	7918	1.00 \pm 0.251 μ s.
3300 pf	$\pm 5\%$	400V	7919	1.49 \pm 0.372 μ s.
4700 pf	$\pm 5\%$	125V	7920	2.10 \pm 0.526 μ s.
6800 pf	$\pm 5\%$	125V	7921	3.03 \pm 0.757 μ s.
0.01 μ F	$\pm 5\%$	400V	7922	4.44 \pm 1.11 μ s.
0.015 μ F	$\pm 5\%$	125V	7504	6.63 \pm 1.66 μ s.
0.022 μ F	$\pm 5\%$	125V	7475	9.72 \pm 2.43 μ s.
0.033 μ F	$\pm 5\%$	125V	7720	14.6 \pm 3.64 μ s.
0.047 μ F	$\pm 5\%$	125V	7044	20.7 \pm 5.18 μ s.
0.068 μ F	$\pm 5\%$	125V	8481	30.0 \pm 7.49 μ s.
0.1 μ F	$\pm 5\%$	20V	9136	44.0 \pm 11.0 μ s.
0.15 μ F	$\pm 5\%$	20V	9915	66.0 \pm 16.5 μ s.
0.22 μ F	$\pm 5\%$	20V	11043	96.8 \pm 24.2 μ s.
0.33 μ F	$\pm 5\%$	15V	9369	145 \pm 36.3 μ s.
0.47 μ F	$\pm 5\%$	15V	NR	207 \pm 51.7 μ s.
0.68 μ F	$\pm 5\%$	15V	9430	299 \pm 74.8 μ s.
1.0 μ F	$\pm 5\%$	15V	9386	440 \pm 110 μ s.
1.5 μ F	NR	15V	----	660 \pm 165 μ s.
2.2 μ F	NR	15V	----	968 \pm 242 μ s.
3.3 μ F	$\pm 5\%$	15V	9431	1.45 \pm 0.363 ms.
4.7 μ F	$\pm 5\%$	15V	9398	2.07 \pm 0.517 ms.
6.8 μ F	$\pm 5\%$	15V	9387	2.99 \pm 0.748 ms.
10.0 μ F	$\pm 5\%$	15V	9309	4.40 \pm 1.10 ms.
15.0 μ F	$\pm 5\%$	15V	NR	6.60 \pm 1.65 ms.
22.0 μ F	$\pm 5\%$	15V	9385	9.68 \pm 2.42 ms.
33.0 μ F	$\pm 5\%$	15V	11044	14.5 \pm 3.63 ms.
47.0 μ F	$\pm 5\%$	15V	11042	20.7 \pm 5.17 ms.
68.0 μ F	$\pm 5\%$	15V	9308	29.9 \pm 7.48 ms.
100.0 μ F	$\pm 5\%$	10V	9151	44.0 \pm 11.0 ms.

% Reduction of delay	0.99	1.4	2.1	3.0	4.5	5.4	6.5	7.7	9.1	12	18
Resistor	47K	33K	22K	15K	10K	8.2K	6.8K	5.6K	4.7K	3.3K	2.2K
% Reduction of delay	24	32	36	41	46	50	59	68	76	82	
Resistor	1.5K	1	820 Ω	680 Ω	560 Ω	470 Ω	330 Ω	220 Ω	150 Ω	100 Ω	

TRANSISTOR PURCH. SPEC. CAT NO.
VT1 PS 21B 1100B

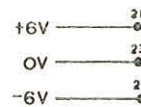
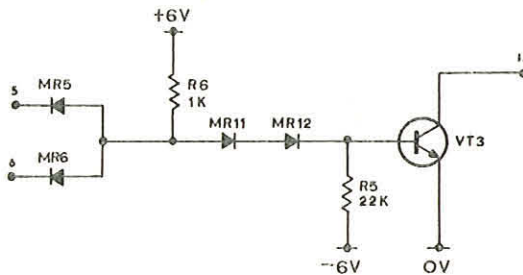
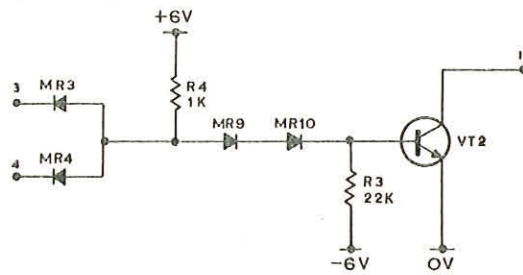
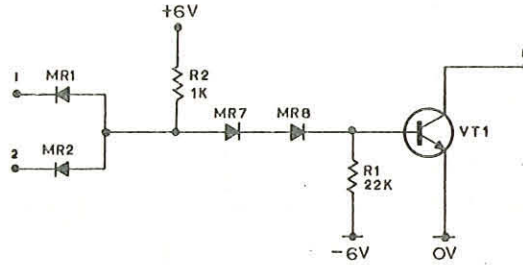
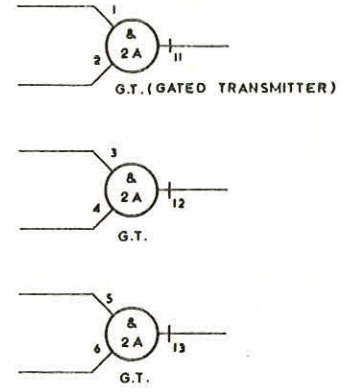
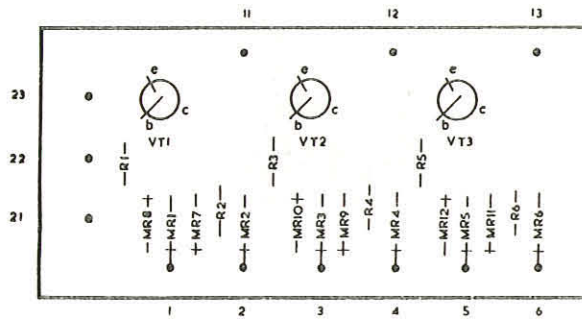


NOTES

1. OUTPUT PULSE POSITIVE.
2. PULSE TRIGGERED BY ANY INPUT REVERTING TO '0' PROVIDED ALL I/P'S HAVE BEEN '1' FOR $\geq \frac{C}{2}$ nS:
(WHERE C = CAPACITANCE IN pF)
3. R3 AND C2 ARE EXTERNAL.
4. IF R3 = 2.7K THEN THE PULSE WIDTH = C nS (WHERE C IS CAPACITANCE OF C2 IN pF) INCREASING VALUE OF R3 INCREASE PULSE WIDTH IN PROPORTION.

INPUT LOGIC LEVELS	
'1'	> 2V
'0'	< 1V

TRANSISTOR PURCH. SPEC. CAT. NO.
VT1-VT3 — 7573



INPUT LOGIC LEVELS	
'1'	= > 2 V
'0'	= < 1 V

TRANSISTOR
VT1- VT3

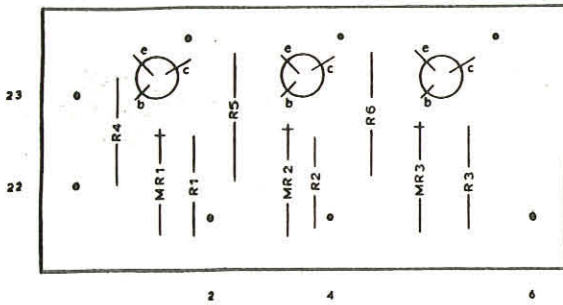
PURCH. SPEC.
PS 218

CAT. NO.
11008

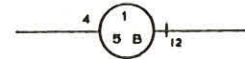
11

12

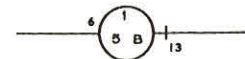
13



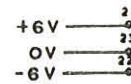
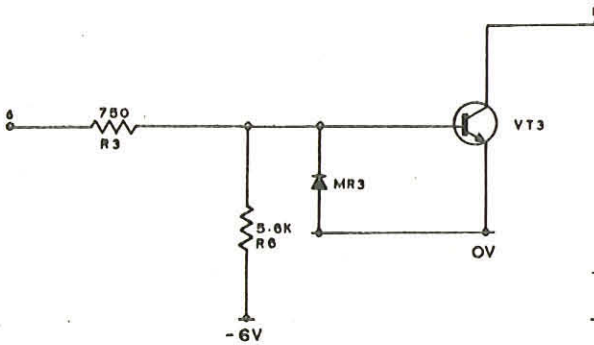
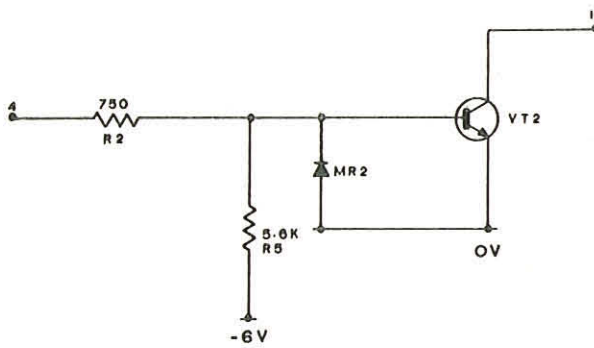
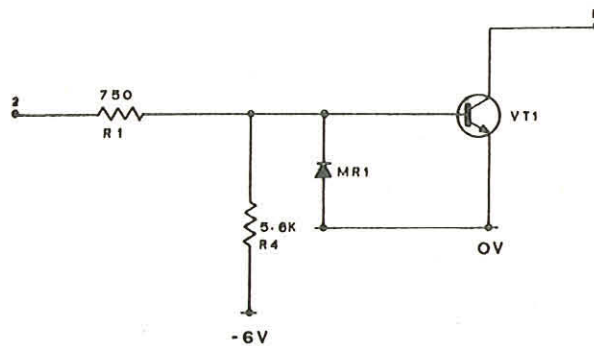
41PR (4100PERIPHERAL RECEIVER)



41PR



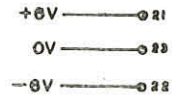
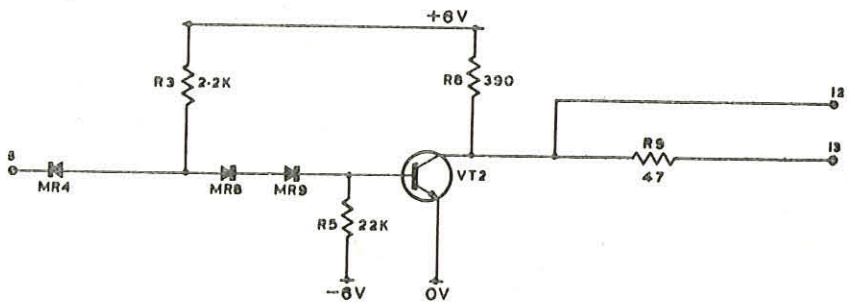
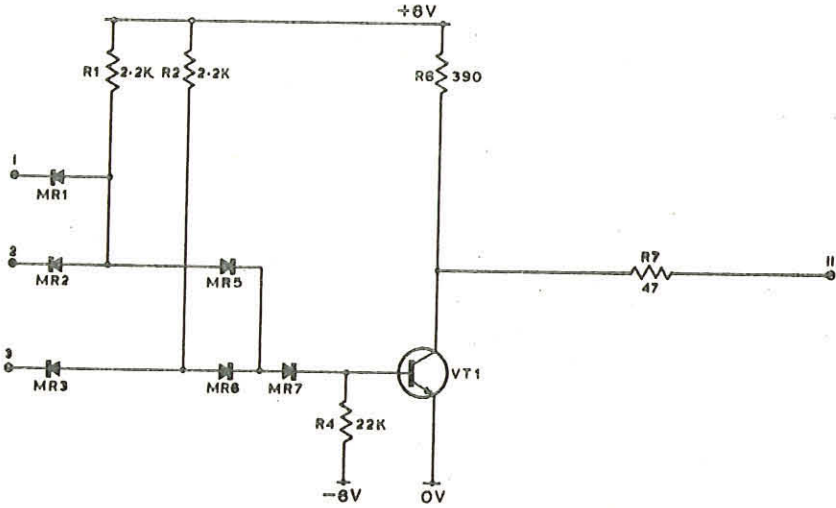
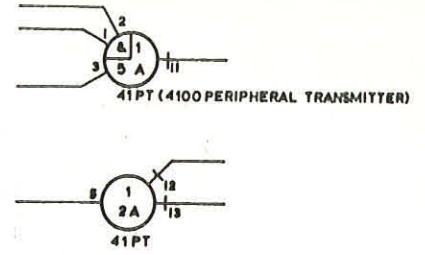
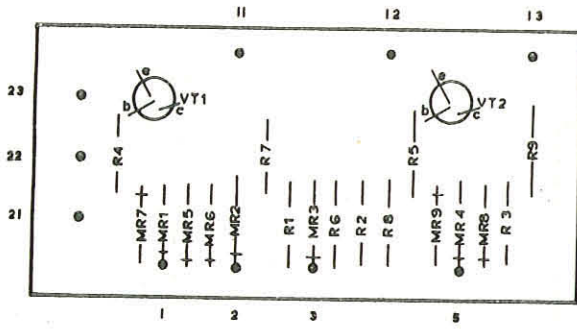
41PR



INPUT LOGIC LEVELS	
'1'	> 3V
'0'	< 1V

4100/900
4.6.1.

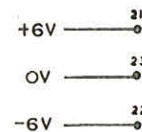
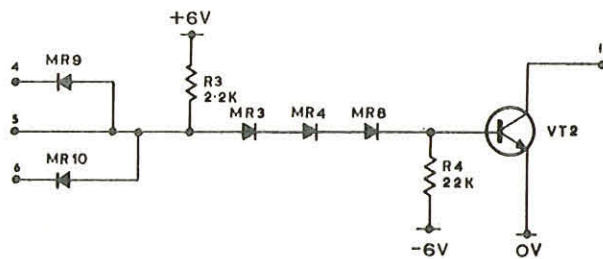
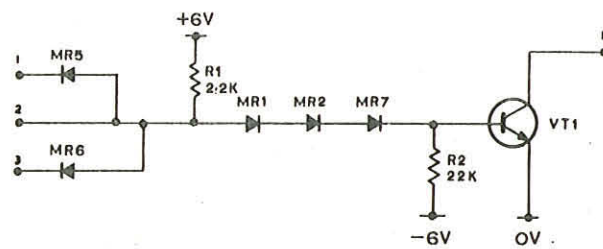
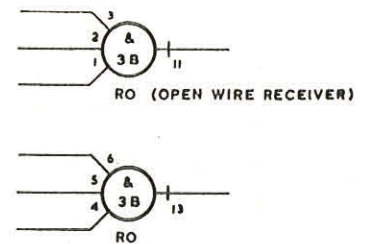
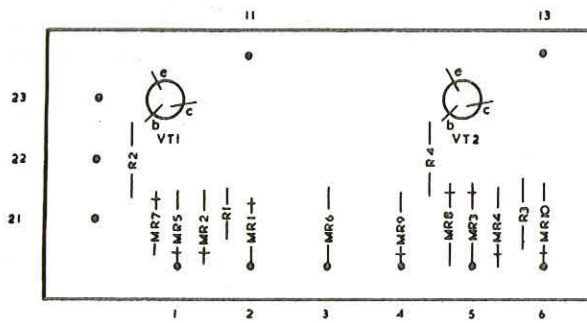
TRANSISTOR. PURCH. SPEC. CAT. No.
VT1, VT2. PS 218 11008



INPUT LOGIC LEVELS	
↑	z > 2V
⊙	z < 1V

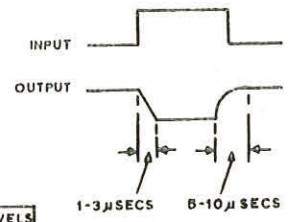
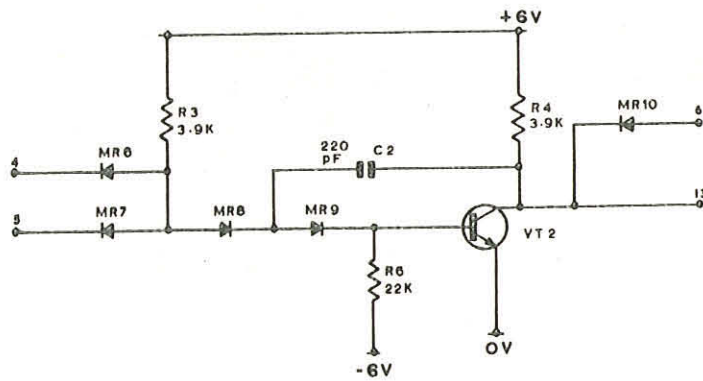
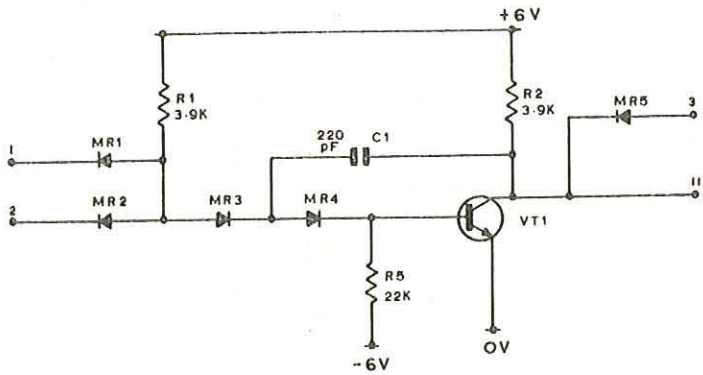
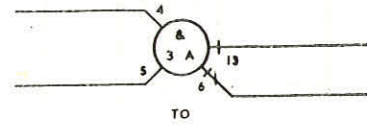
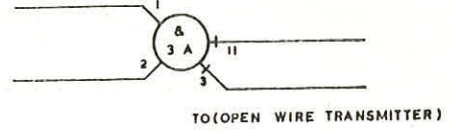
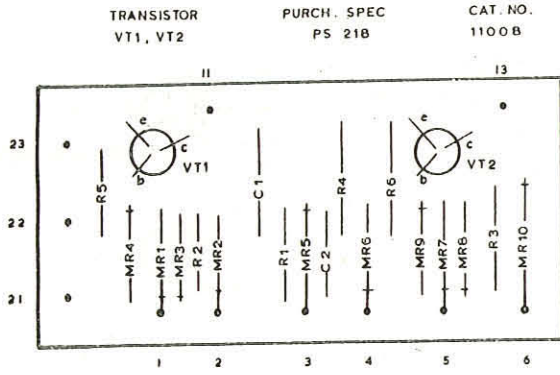
Figure 48 (ISSUE 2)

TRANSISTOR PURCH. SPEC CAT. NO.
VT1, VT2 PS 21B 1100B



NOTE
INPUTS 1,2 AND 4,6, USED WHEN RECEIVING
FROM BUS INPUTS 2 AND 5 OTHERWISE

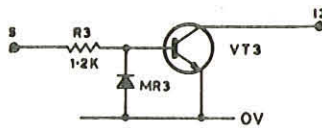
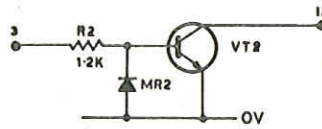
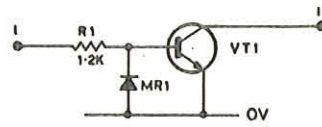
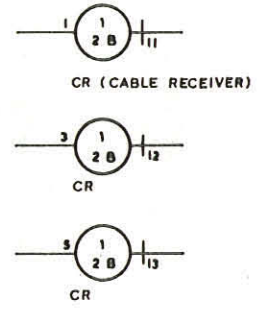
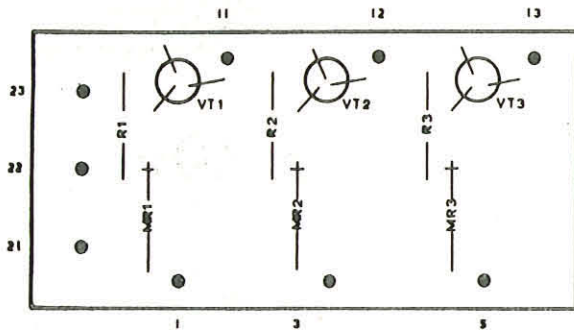
INPUT LOGIC LEVELS	
'1'	= > 2.5V
'0'	= < 1.5V



INPUT LOGIC LEVELS
'1' = > 2 V
'0' = < 1 V

NOTE:-
 OUTPUTS 3&6 USED WHEN DRIVING
 ON TO BUS. OUTPUTS 11&13 USED OTHERWISE.

TRANSISTOR PURCH. SPEC. CAT. No.
VT1-VT3 PS 218 1100B



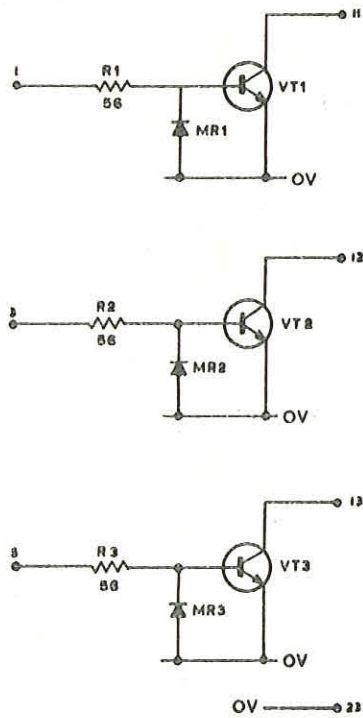
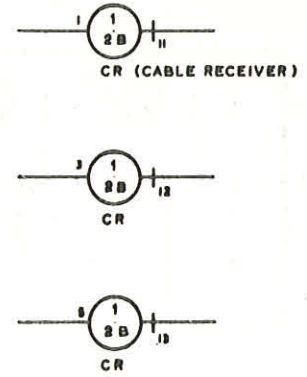
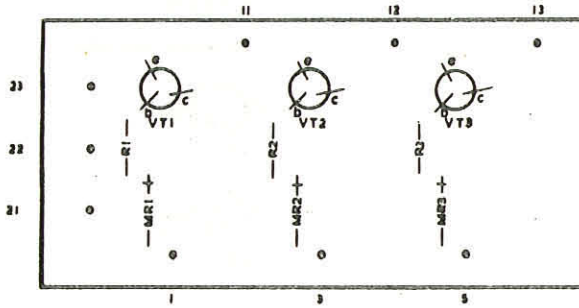
NOTE:-

USED IN CONJUNCTION WITH A SINGLE FAST
CABLE DRIVER LSA12G FEEDING BUS
OF RECEIVERS.

INPUT LOGIC LEVELS	
'1'	$\geq 2V$
'0'	$\leq 1.5V$

4100/900
4.6.1.

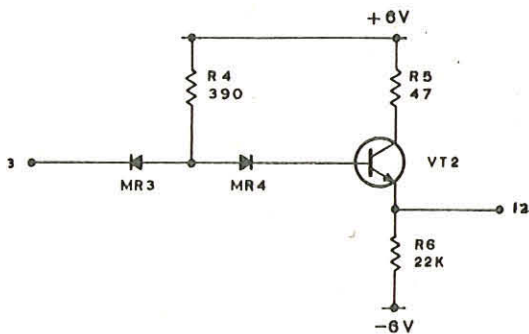
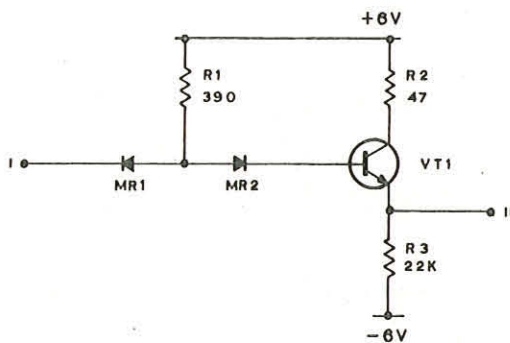
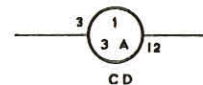
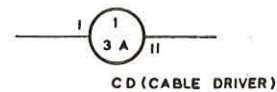
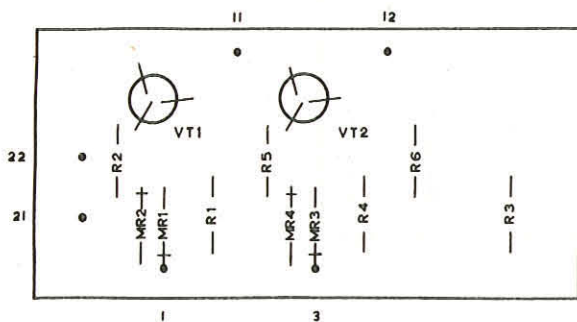
TRANSISTOR PURCH. SPEC. CAT NO.
VT1-VT3 PS 218 11008



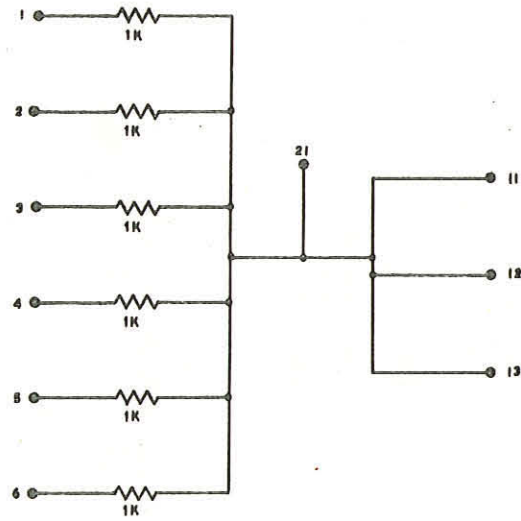
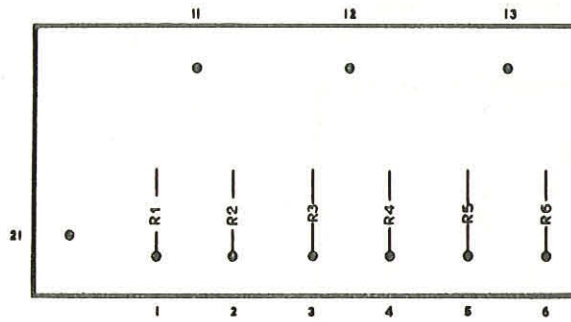
NOTE:
USED IN CONJUNCTION WITH A BUS OF FAST CABLE
DRIVERS L.S.A. 126 FEEDING A SINGLE RECEIVER.

INPUT LOGIC LEVELS	
V ₁ '	= > 2V
V ₀ '	= < 1.5V

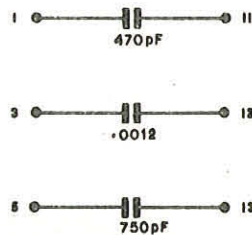
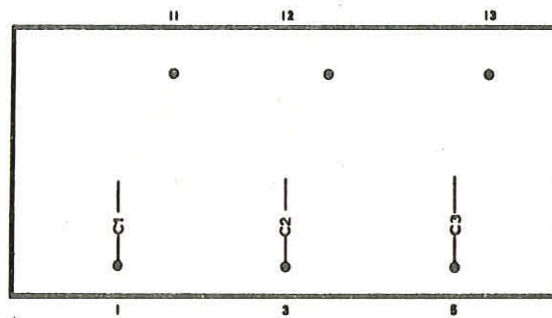
TRANSISTOR PURCH. SPEC CAT NO.
VT1, VT2 PS 218 1100B



INPUT LOGIC LEVELS	
'1'	= > 3.5V
'0'	= < 1V



LSA.132



LSA.133

TRANSISTOR CAT. No.
VT1-VT3 11740

